A Study of Full Adder Circuits: from Power and Speed of Operation Perspective

Manoj Duhan[1], Kusum Dalal[2], Viplove Kumar[3]

[1,2]Faculty member, Department of ECE, DCRUST Murthal
[3] Research Scholar, ECE Dept., DCRUST Murthal

ABSTRACT: ***In this paper, we review various design techniques for full adder circuits as these circuits are basic building blocks of many arithmetic circuits. Different techniques are used for low power in full adders. Analysis is based on some simulation parameters like number of transistors, power, delay, power delay product and different technologies at different supply voltages. This paper contributes to a better knowledge of the behaviour of conventional CMOS and CPL full-adder circuit when low voltage, less delay, low power or small power delay products are of concern. This paper will help the circuit designers to select the full adder that satisfies their application***

KEYWORDS: Full Adder, Dynamic circuits, Power-delay products (PDP), Very Large Scale Integration Circuits, Hybrid XOR-XNOR circuits, Bridge full adder.

1. INTRODUCTION

The development of low power circuits faces tremendous challenges as service increases. These challenges, led to tremendous growth in research that specially target on development of low power synthesis tool. Addition is one of the most basic and fundamental operations that describe whole performance of system. The performance of many applications such as digital signal processing depends upon the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation, and digital filtering. Especially regarding the development of mobile systems such as portable computers and cell phones, many researches are being dedicated to high speed, low power circuits. Consequently, as a critical part of digital processors, adders are largely studied. The general trend of increasing operating frequencies and circuit complexity, to compensate with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits [1-7].

The main task of a full adder is to add two binary numbers and it serves the nucleus of many other useful operations. In most of these systems the adder lies in the critical path that determines the overall system performance. That is why enhancing the performance of binary adders is a significant goal. The 1-bit full adder cell is the building block of binary adders. Enhancing its performance implies enhancing the performance of the whole system.

2. LITERATURE SURVEY OF FULL ADDERS

2.1 Conventional CMOS Full Adder

Conventional CMOS Full Adder is the most basic full adder implementation techniques. Conventional CMOS Full Adder consists of 28 transistors. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs [7]. This circuit uses both NMOS and PMOS transistors. In Conventional CMOS Full Adder, there are many leakage paths which lead to more sub threshold leakage [10]. Now a days the size of devices are shrinking and the power supply is rapidly reduced, so power consumption becomes critical. Conventional CMOS is the most stable and robust full adder [8]. In standby mode the leakage power plays a vital role in the total power consumption and we should reduce this leakage power. The best way of reducing the leakage power dissipation of s VLSI circuits in the STANDBY state is to remove its supply voltage [10].

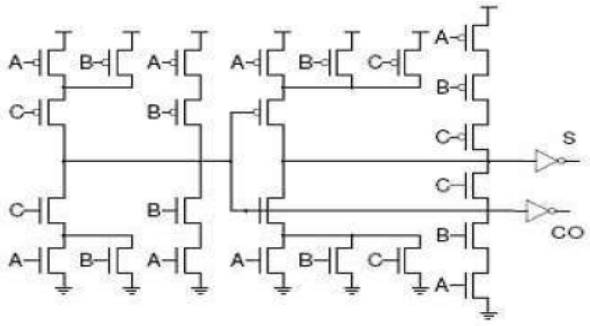

Figure 1. Conventional CMOS Full Adder [7]

2.2 Transmission Function Full Adder

Transmission Function Full Adder is one of the full adder implementation techniques. Transmission function full adder consists of 16 transistors. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs. This circuit uses both NMOS and PMOS transistors [2, 7]. There is no voltage drop problem but it requires double the number of transistors to design the function. This full adder is low power consuming but they are good for designing XOR and XNOR gates [2]. Lack driving capability is the main disadvantage in this logic style, more numbers of transistors are required. If TGA and TFA are cascaded, their performance degrades significantly [7]. It also have lower loading of the inputs and intermediate nodes, lower transistor count and balanced generation of Sum and C_{out} signal.

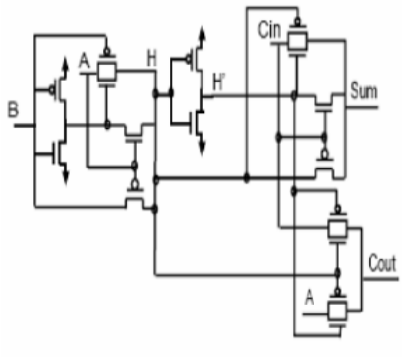

Figure 2. Transmission Function Full Adder [7]

2.3 10T Full Adder

Kevin Navi, Mehrada Maeen, Vahid Foroutan, Somayeh Timarchi and Omidkavehei says that Full adder using 10T uses more than one logic style for the implementation and it is called as Hybrid logic design style. The number of transistors count is 10. A, B and C_{in} are the inputs and Sum & C_{out} are the outputs. Full Adder using 10T cannot work under 1V, which results in the supply voltage of 1.8 V. 10T generates A XOR B and use it along with its complement as a select signal to generate the output. In full adder 10T small number of transistors count are used and produces the non full swing pass transistor with the full swing restored transmission gate technique. 10T has the smallest delay because of its supply voltage. It produces high capacitance values for the inputs; this is the only disadvantage in full adder 10T [2]. 10T have lower loading of the inputs and intermediate nodes, lower-transistor count and balanced generation of Sum and C_{out} signal.

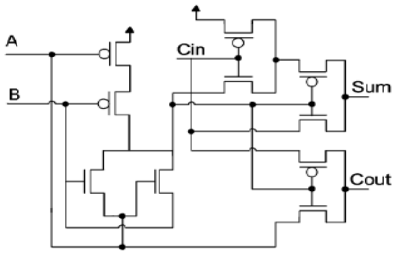

Figure 3. 10T Full Adder [2]

2.4 Transmission Gate Full Adder

Reza Faghih Mirzaee, Mohammad Hossein Moaiyeri and Keivan Navi say that Transmission Gate Full Adder (TGA) is one of the full adder implementation techniques. TGA circuit is based on transmission gate. Transmission gate full adder consists of 20 transistors. TFA consists of a PMOS transistor and NMOS transistor that are connected in parallel way, which in particular type of pass transistor logic circuits. A, B and C_{in} are the inputs and Sum and C_{out} are the outputs. There is no voltage drop problem (full swing) but it requires double the number of transistors to design the function. It consumes low power therefore it is good for designing XOR or XNOR gates [2]. The main disadvantage of this logic style is that it lack driving capability, more transistors are needed i.e. more complexity and capacitance. When TGA are cascaded, their performance degrades significantly.

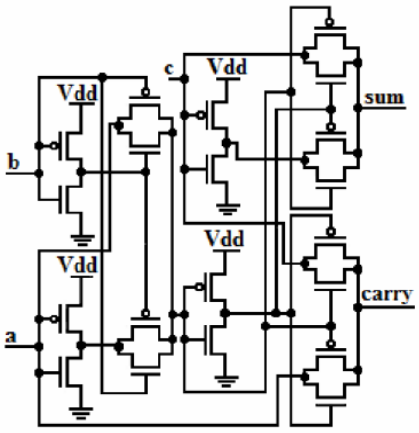

Figure 4. Transmission Gate Full Adder [2]

2.5 14T Full Adder

Dr. P. T. Vanathi, Dr. J. Ramesh, K. Revathy, R. Preethi, C. Haritha Laxmi and K. Keerthana say that 14T full adder consists of 14 transistors to generate the sum and carry. The adder consists of four transistor XOR structure, four transistors XNOR structure and an inverter. Sum is generated using pass transistors logic and carry is generated using transmission gate logic. XOR gate and its complementary signals are derived using an inverter and it also act as gate control signals for both transmission gates which exist in the carry path. The inverter in the path causes dynamic power dissipation. Advantages of 14T full adder are better cascading capability, low power consumption and higher operating frequency [1,2].

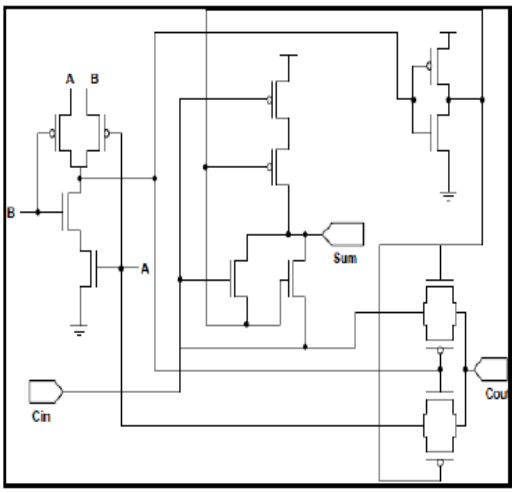

Figure 5. 14 T Full Adder [2]

2.6 SERF Full Adder

SERF adder reuses charge by the energy recovering logic and hence consumes less power than non-energy recovering logic. SERF adder has no direct path to the ground, therefore power dissipation is reduced. The charge stored at the load capacitance is reapplied to the control gates. The joint effect of these two things makes the SERF adder an energy efficient design. Disadvantage of SERF adder is that it does not provide full-swing for the internal nodes, as the power consumption by the circuit reduces the circuit becomes slower [13]. Also it cannot be cascaded at low power supply due to multiple threshold problems.

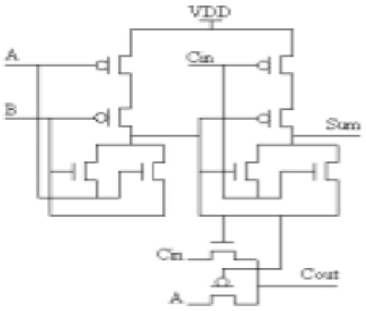

Figure 6. SERF Full Adder [13]

2.7 Gate Diffusion Input Full Adder

A. Bazzazi and B. Eskafi says that Full adder cell with the GDI technique is implemented to design a high performance and low power full adder. GDI cell contains three inputs- G (common state input of NMOS and PMOS), N (input to the source or drain of NMOS) and P (input to the source or drain of PMOS). Full adder cell comprises of 10 transistors. The only state where low swing occurs in the input value is A=0, B=0. In this case, the voltage level of F1 is V_{tp} (instead of the expected 0 V) because of the poor high to low transition characteristics of the PMOS pass transistor [2,11]. In some cases, when V_{dd}=1 without a swing drop from the previous stages, a GDI cell functions as an inverter buffer and recovers the voltage swing, although this feature allows a self-swing restoration in certain cases [11].

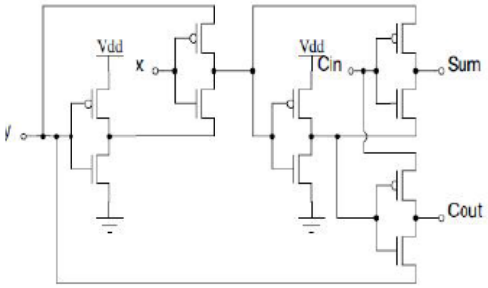

Figure 7. Gate Diffusion Input Full Adder [11]

2.8 P-XOR and G-XOR Based Full Adder

It resembles the inverter-based XOR but the difference is that the VDD connection in the inverter-based XOR is connected to the input A. Since the new XOR gate has no power supply, it is called Powerless XOR, or P-XOR. A new XNOR gate is named as Groundless XNOR or G-XNOR because there is no direct connection with ground. 9B and 13A are the adders which are implemented using this technique. The addition of 2 bits A and B with C_{in} yields a Sum and C_{out} bit. These adders are having low power consumption and better speed performances. The basic disadvantages of these full adders are that it suffers from the threshold-voltage loss of the pass transistors. They all have double threshold losses in full adder output terminals. This problem usually restricts the full adder design from operating in low voltage or cascading without extra buffering.

2.9 Complementary Pass Transistors Full Adder

The CPL Full Adder has 18 transistors and is based on NMOS pass-transistor logic. This causes low input capacitance and high speed operation. However it also leads to threshold voltage loss in the output circuit. CPL consumes less power than standard static CMOS circuits, due to less output swing. However it reduces noise margin and causes serious problems in cascading, especially in low voltages. Therefore, CMOS inverters are used to restore the outputs voltage level and ensure the drivability, and feeble PMOS transistors are used to minimize the static current caused by the incomplete turn-off of the PMOS in the output inverter. The advantages of the CPL style are the small input capacitance, low internal voltage swing, good output driving capability due to the output inverters, and a fast differential stage due to the cross-coupled PMOS pull-up transistors [5,7,9]. Disadvantage of CPL is that two MOS networks are required. Due to the presence of a lot of internal nodes and static inverters, there is large power dissipation [7].

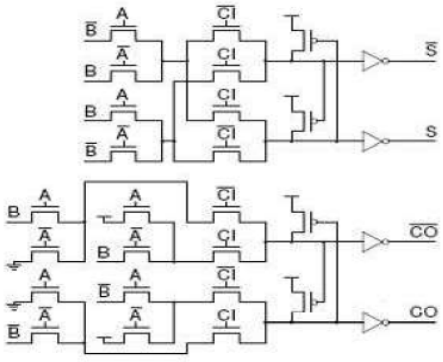

Figure 8. Complementary Pass Transistors Full Adder [7]

2.10 8T Full Adder

Vahid Foroutan, Keivan Navi and Majid Haghparast say that 8T full adder is implemented using Majority Function. The majority function is a logical circuit that performs a majority vote to determine the output of the circuit [7]. It uses three input capacitances in order to implement different functions with unique circuit implementation. The threshold voltage is reduced to make the pre-discharge circuit working. This reduction in V_{th} influenced the performance of the circuit, but at the same time lower power dissipation is gained. Input capacitances influence the speed of the circuit. In order to maintain the performance of the circuit, we have to reduce the number of the input capacitances. The delay of the circuit is reduced due to the lower input capacitances, meanwhile the power consumption of the circuit is low, leading to a better Power-Delay-Product [7].

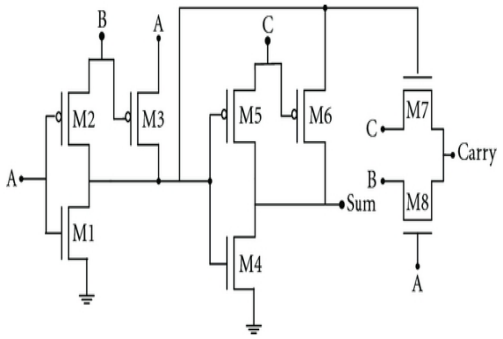

Figure 9. 8T Full Adder [7]

3. COMPARATIVE STUDY OF DIFFERENT FULL ADDER TECHNIQUES

Design	Power (uW)	Delay (ns)	PDP (fJ)	No. Of transistors
CMOS	2.747	0.133	0.365	28
CPL	4.013	0.129	0.521	18
TFA	3.035	0.132	0.402	16
TGA	3.066	0.134	0.412	20
10T	0.761	1.331	1.331	10
GDI	0.952	0.266	0.253	10
8T	1.185	0.166	0.197	8
14T	1.993	0.737	1.468	14
SERF	4.941	0.373	1.842	10
9B	5.486	0.054	0.297	10
13A	5.560	0.035	0.197	10

Table 1. Comparison of different full adders on the basis of Power, Delay, PDP and Transistor Count [1-9, 11, 13]

3.1 Power Comparison

SERF suffers from lacking proper driving capabilities in cascaded operation, takes much longer time to accomplish the computation therefore it have low speed of operations as a result higher power dissipation. 13A and 9B full adder suffers from threshold voltage loss of pass transistor as a result it dissipate more power. CPL adder dissipates more power due to dual-rail structure and higher number of internal nodes. TFA and TGA have less transistor count but due to the lack of drivability, additional buffers are required at each output, which

increase their short circuit power as well as switching power. 10T full adder is best among all with respect to power dissipation. GDI full adder is fastest with lowest power consumption. 8T dissipates less power because of its transistors count. 14T is mostly used by the designers as it has best driving capability and also it works on low voltage and power dissipation is low.

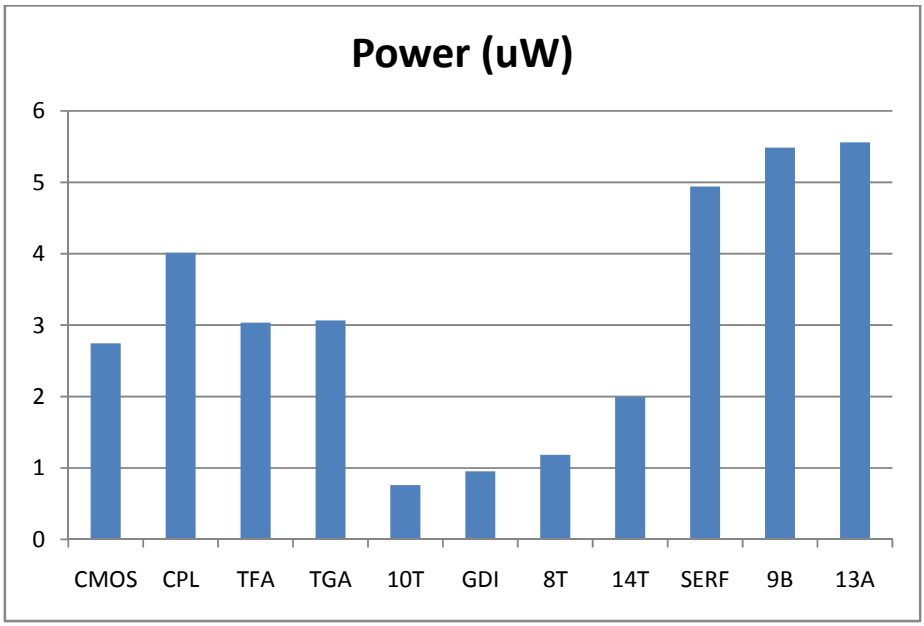

Figure 10

3.2 Delay Comparison

13A and 9B have almost same delay and better delay as compared to SERF full adder. In gate diffusion input full adder, buffers are added after every cell for swing restoration. This prevents voltage drop, but the payment will be in additional area, delay and power dissipation. CPL full adder has the nominal delay. TGA uses CMOS transmission gate logic similar to static CMOS full adder. The 8T dynamic full adder is slower than complementary dynamic CMOS full adder. 14T full adder, TFA and SERF are the only full adders which are linear.

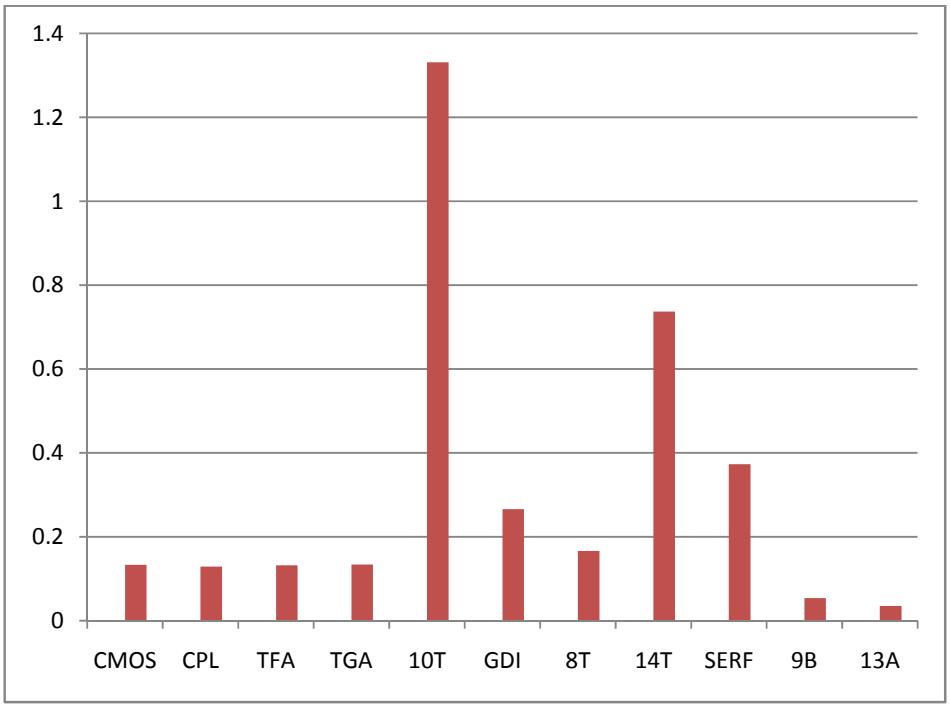

Figure 1

3.3 PDP comparison

The PDP is a quantitative measure of the efficiency of the trade off between power dissipation and speed. This parameter is very important when low power operation is needed. The 8T has the best PDP in comparison with the others. SERF, TGA, CPL and 14T full adders show almost similar results because they have almost critical delay. 13A, 9B, 10T and GDI full adder shows almost similar results because of lower internal nodes and having same transistor count. TFA have higher PDP because there are higher internal nodes which increase capacitance and wire complexity. As a result power consumption and time delay increases and power delay product also increases.

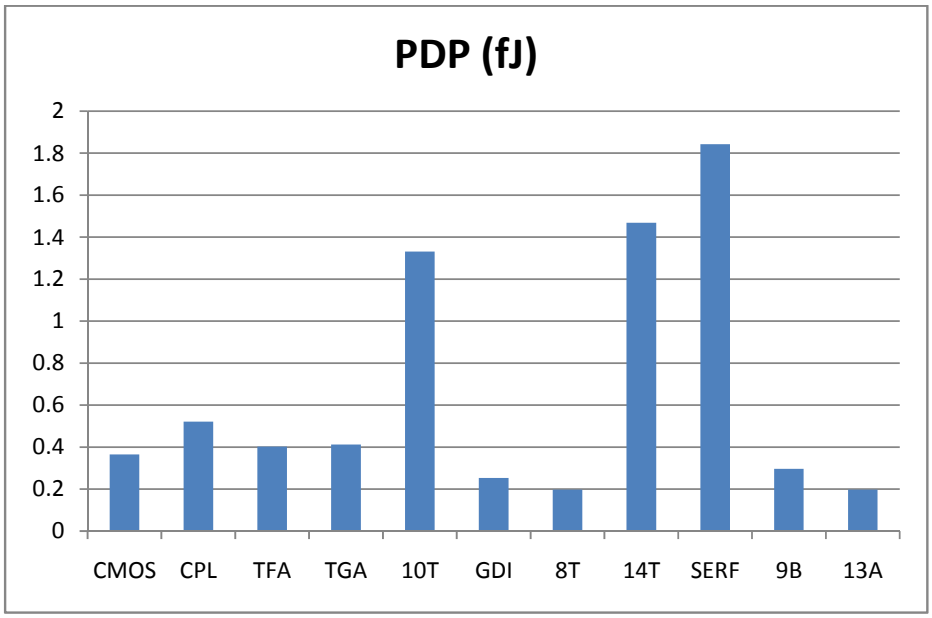

Figure 12

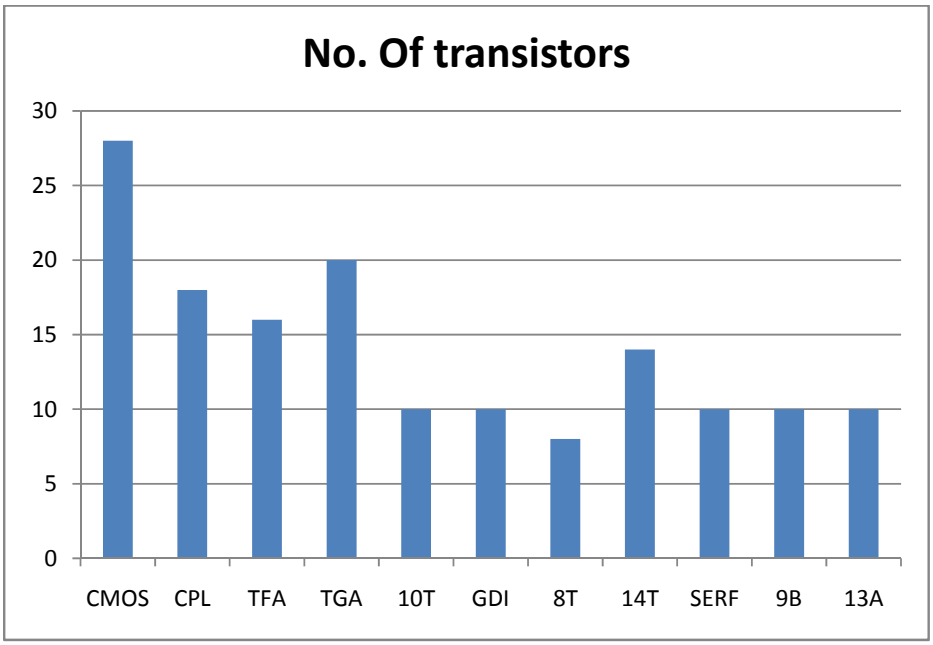

Figure 13

4. CONCLUSION

In this paper, various types of full adder cells designs have been reviewed from the most recent published research work. This paper shows comparison of full adder cells with each other in term of power, delay, PDP and transistors count is done as shown in figure 1,2,3 and 4. Different methods and logics are used in this paper to build the full adder to reduce the power, delay, power delay product (PDP) and transistor count. Based on survey 8T consume less power, power delay product (PDP), delay and transistor count compare to all other

designs at low supply voltage. This circuit is suitable for VLSI application with very low power consumption and delay. A widely comparison of adder cells design with the help of Cadence tool for VLSI Design illustrates a significant improvement in terms of power dissipation and PDP. Switching activity is reduced significantly due to reduction in number of transistors. Also, due to its dynamic characteristics, short circuit current is eliminated. Therefore the best PDP in adder circuit is attained by reducing power dissipation as well as by enhancing the operational speed of specific design.

5. REFERENCES

[1]Dr. P.T. Vanathi, Dr. J. Ramesh,K. Revathy, R. Preethi, C. Haritha Laxmi and K. Keerthan, "Performance Analysis of High Performance Adder Architectures" ,Volume 2, Issue 1, 2012

[2] G. Sathiyabama, Raja Shailaja," A Survey of Low Power High Speed Full Adder", International Journal of Emerging Technology and Advanced Engineering, Volume 2, Issue 9, September 2012

[3] Subodh Wairya, R. K. Nagaria, Sudarshan Tiwari," New Design Methodologies For High-speed Mixed-mode CMOS Full Adder Circuits", International conference of VLSI design & communication Systems, Volume 2, No. 2, June 2011

[4]Shivshankar Mishra, V. Narendra, Dr. R. A. Mishra, "On the Design of High Performance CMOS 1-Bit Full Adder Circuits", International conference on VLSI, Communication & Instrumentation, Volume 5, Issue 2

[5] M. H. Moaiyeri, R. F. Mirzaee and K. Navi, "High Speed NP-CMOS and Multi-output Dynamic Full Adder Cells", International Journal of Electrical and Electronics Engineering, Volume 4, Issue 4, 2010

[6] K. Navi, M. Maeen, V. Foroutan, S. Timarchi, and O. Kavehei, " A Novel low-power Full Adder cell for low voltage", Integration, the VLSI Journal, Volume 42,issue 4, 2009

[7] Vahid Foroutan, Keivan Navi and Majid Haghparast," A new Low Power Dynamic Full Adder Cell Based on Majority Function", World applied science journal, Volume 4, Issue 1, 2008

[8] K. Navi and O. Kavehi, "Low-power and High-performance 1-Bit CMOS Full Adder Cell, Journal of Computers, Volume 3, Issue 2, 2008

[9] J. M. Quintava, M.J. Avedilla, R. Jimenez and E. Rodriquez-Villegas," Low Power Logic Styles for Full Adder Circuits", 8th IEEE International Conference on Electronics, Circuits and Systems (ICECS'01), Malta 2001

[10] N. Weste and K. Eshraghian, "Principles of CMOS VLSI design, A System Perspective", MA: Addison-Wesley, 1993.

[11] A. Bazzazi and B. Eskafi," Design and Implementation of Full Adder Cell with GDI Technique Based on 0.18um CMOS Technology", Volume 2, 2009

[12] Zhengming Fu, Jian Xu, "Cadence User Tutorial", Version 1.2 September 18, 2004

[13] R. S. Halem, E. John and L. K. John," A Novel Low Power Energy Recovery Full Adder", National Science Foundation, Grant number ECS-9714993