A REVIEW: FIR FILTEROPTIMIZATION USING MCM AND CSE METHOD

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Abstract- Complexity of many digital signalprocessing (DSP) systems reduced by aMultiple Constant Multiplication (MCM)operation. For the better performance of digital signal processing systems, Multiple Constant Multiplication (MCM) operation is not sufficient. To get better results some other operations are used with MCM. Thus, this paper introduces a Common Sub expressionElimination (CSE) operation with MCM operation. With the help of these techniques problems in the optimization of finite impulse response(FIR) filter design can be solved by decreasing the number of operators. Using These Techniques show the efficiency by reducing area when compared to previously used algorithmsdesigned.

Keywords-FIR, MCM, CSE, CSD, BSD

1. Introduction

FIR filters are inherently stable and require no feedback. Major factors that influence the choice of a specific realization are computational complexity, memory requirements and finite word length effects.Filter optimization is the process of designing a signal processing filter that satisfies a set of requirements. The purpose is to find optimization of the filter to acquire each of the requirements to make the filter sufficient stable and useful. Optimization of FIR filters are done by reducing the area, power etc by using different algorithm. Area is reduced by minimizing the number of addition/subtraction operators. This can be only done by using MCM and CSE Techniques. The multiple constant multiplication (MCM) is defined as a technique to find out the minimum number of addition and subtraction operations required for the multiplication of multiple constants by an input variable. The CSE is defined as a technique to find out the minimum number of addition and subtraction operators by taking operators as common.

2. Algorithm

Multiplier Constant Multiplications is a straightforward way of realizing the constant multiplicationsunder a shift-adds architecture. [6] It is first to define the constants under a particularnumber representation, and second, for the nonzerodigits in the representation of the constant, is to shift the inputvariable according to thedigit positions and add/subtractthe shifted variable with respect to the digit values. As asimple example, consider the constant multiplications 29xand 43x.Their decompositions in MCM are listed as follows [8]

29x= (11101) bin x=x<<x+2<<x+3<<x+4

43x= (101011) bin x=x<<x+5<<x+3<<x+1

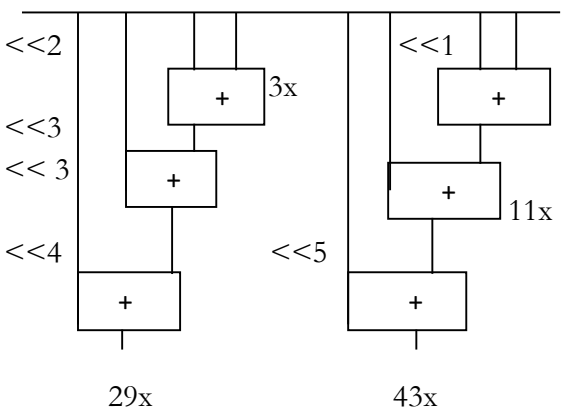

Fig 1.MCM (6 Adders)[3]

In CSE, take 101 and 11 as common, to reduce the number of operators.

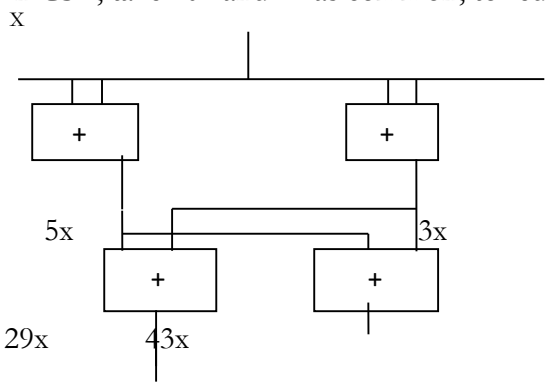

Fig 2.MCM with CSE (4 Adders)[3]

3. Previous Work

To reduce the number of operators, firstly use a Common Sub expression Elimination (CSE) algorithm with a based on the Canonic Signed Digit (CSD) representation of filter coefficients for implementing low complexity FIR filters.[7] In Canonical signed digits it's difficult to deal with "+" and "-"[1]. Thus a Multiple constant multiplications were represented using the binary signed digit number(BSD) system which gives a better performance over Canonical Signed Digits (CSD).In BSD, each digit associated with a sign,+ve or –ve.

For Example,7 is represented as 0111 in binary form. By using BSD

(1 0 -1 1)=8-2+1 ; (1 0 0 -1)=8-1

Thus BSD show Redundancy [4]. Without deal with digits, Digit-serial MCM design is used that offers alternative low complexity MCM operations at the cost of an increased delay. In digital-serial, processing will be bit by bit. So more time is required. It was a Tradeoff between time and Area [3].After this, a use of MCM with Adder graph which reduces more the no of operators but there is no rule in adder graph to common block which create difficulty and take more time to solve the problem[2]. To overcome this problem, bits based adder tree are used in algorithm.

AAdder Tree by Greedy Scheduling Algorithm and Bit Level resource optimal adder tree are used to minimize the number of operators or to minimize the height of a adder tree by using less number of operators.

For Example,x

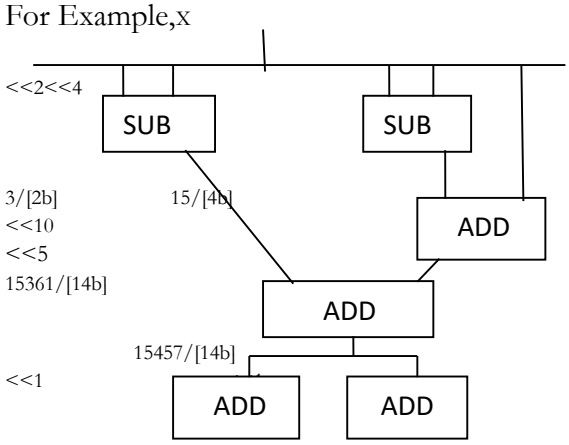

Fig 3. Adder Tree by greedy scheduling algorithm [5]

x

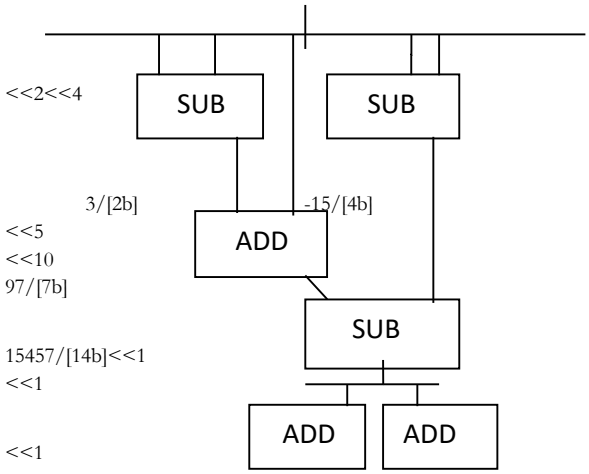

Fig 4. Bit Level resource optimal adderTree [5]

Both have same procedure but the difference is that second layer of tree has only 7 bits in bit level as compared to 14 bits are in greedy scheduling algorithm. This wider bit width signal require higher hardware cost when input is given to next layer of operators.Secondly,subtractions with shift reduces the cost of hardware. In Bit Level more number of sub tractor operators are used as compared in greedy scheduling algorithm [5].Further, it is observed that MCM had been on more effective common sub expression elimination, which sum up the computed sub-expressions for each coefficient, largely omitted.

4. Conclusion

Various methods for reducing the area are studied from research and review papers. The principle reason for the reducing area is optimization of FIR filters. It can be done by using efficient Techniques MCM and CSE which gives the better performance of FIR filters. These techniques will help in reducing the area by using less number of additions/subtract operators. If the area will decrease then it's easy to deal with large system where numbers of filters are used. By reducing area system will become more reliable.

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