A Low Power 16 Bit Vedic Divider for High Speed VLSI Applications

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Abstract. This paper proposes the implementation of a low power and high speed Vedic Divider based on ancient Indian Vedic mathematics. In this paper, an algorithm based on the "ParavartyaYojayet" is applied, throughout this sutra the propagation delay and power consumption are reduced to an extent. As considered, division operation is more complex in the computation of the digital applications. The most significant aspect of thispaper is to reducethe power consumption and provide high speed. In this work decimal and binary number division algorithms are performed. Synthesis results are calculated on Tanner EDA Tool 13.0 at 32nm technology. The simulated results for proposedVedic divider shows a reduction in delay and power consumption against other division methods.

Keywords: Paravartya sutra, Vedic divider, Binary division.

1. Introduction

A mathematical process of splitting a number into equal parts or groups, it is the process of being separated called division. Divider is basic hardware employs in high speed and advanced digital signal processing (DSP) units.Its most important role in high precision radar technology, cryptography and linear predictive coding (LPC) for speech processing [2]. As the technology shrink, dividers perform an important role in every field like cloud data storage, speech processing, payment through NFC. Digital signal processing is the area where fast processing of bits required, so faster algorithms are introduced. In comparison to other mathematical operations, division is the sequentional type of operation that results in complex hardware implementation. The highly accuratedivision algorithms are the basic requirement in real-time signal and image processing applications [10]. The different division architectures are developed to reduce the computational difficulties.The SRT(Sweeny Robertson and Tocher) division,Newton Raphson Method and Long Division Method are the most widely used division techniques.SRT division is the digit recurrence algorithm, where input operands are the floating point n bit with sign-and-magnitude representation. Newton Raphson method is applied when a series of equations in the damping infinitesimal steps take place. Another most common technique is restoring division in which repetitive digit method is used by which digits are added back or restored to remainder adder. This design approach accurately speeds up operation and faster to implement.

2. Related Work

Low power Vedic divider was proposed in [3] provides 27.393ns delay,34% reduction in latency and less power consumption in comparison to conventional design. Vedic divider was provided high operationalspeed. In [5] author presented the design of Vedic divider optimizedbinary division using Vedic "Paravartya and Nikhilam "sutra. Divider operation provided 14.452ns delay that was 19% less than conventional method.The design was coded in Verilog, synthesized and simulated using Xilinx ISE design suit 14.2.

High speed Vedic divider using "ParavartyaYojayet" sutra was proposed in [8]. Functionality of divider was provided 34mw power consumption for LUT utilization of 23/1536 and resulted delay was 19.9ns. It showed that propagation delay and power consumption were reduced significantly.
In [10] a high performance divider was proposed for VLSI applications.Proposed work provided 109mw power consumption against conventional divider. The design was synthesized using 32nm standard cell libraries.

3. Vedic Mathematics Algorithm

The Vedic mathematics has unique techniques based on sixteen sutras. The computational methods using Vedic algorithms are easy to implement and fast in processing. These sutras reduce the iterations for complex circuitry. Division is carried out using Paravartya sutra.

3.1. ParavartyaYojayet (Transpose and Apply)

Division algorithm for decimal numbers is implemented based on "Paravartya-Yojayet – Transpose and Apply" see in table 1. Decimal division provides easier andlogically simple implementation as illustrated using an example [3].

Table 1. Vedic Division using 'PY' sutra

Divisor	Dividend
1 2 3	1 3 5 6 7
- 2 - 3	- 2-3
	- 2 - 3
	0 0
	1 1 0 3 7
	Q=110 R=37

Assume 13567 as the dividend and 123 as the divisor inputs. Allthe divisor inputs are complemented except the most significant bit according to sutra. These complemented divisor inputs are multiplied to addition results of each column of the dividend. At First, MSB dividend bit is partially multiplied with complemented digits of divisor, multiplication results are added with next dividend input and.The quotient and remainder results are carried out using successive addition of columns. In repetitive subtraction method the number of iterations is 124, while as in Vedic technique, the number of iterations reduced to 8.

4. Modified Vedic Divider Architecture

4.1. 8 by4 bit Vedic divider

The modified Vedic algorithm is elaboratedusingeight dividenddata inputs and four divisor data inputs see in table 2. As per Paravartyasutra,MSB bit of divisor is neglected and remaining bits are complemented.

Table 2. Vedic algorithm for 8 by 4 bit Division

Divisor	Dividend
0 1 1 0	1 0 1 1 0 0 0 0
- 0 -0 1	- 0 -0 1
	0 0 0
	- 0 - 0 1
	0 0 0
	- 0 - 0 1

	1 0 - 1 0 1	1 0 1
	Q=10001-110	R=101
	Q=10111	

The modified Vedic divider hardware block consists A0A1A2A3A4A5A6A7 as dividend digits and B1B2B3 as the divisor digits see in fig.1.At first, A0 is partially multipliedwith complemented divisor digits B1, B2 and B3. Multiplied data added with dividend input A1 and then again summation results are multiplied withcomplemented divisor digits.The each successive additionresult is used as one of the multiplicand for further partial multiplication.This cycle repeats until addition results for A7 are carried out. During addition carries generates from one row propagates to next row and so on as per sutra. In this operation, find one negative number take first complement on this numbers and then subtraction takes place. The addition results are carried out through full and half adders while as AND operation is carried out through AND blocks. Output quotients Q0Q1Q2Q3Q4 are consider in eq.(5) to eq. (9) and remainders in eq.(10) to eq.(12). Final quotient consider in eq.(13).

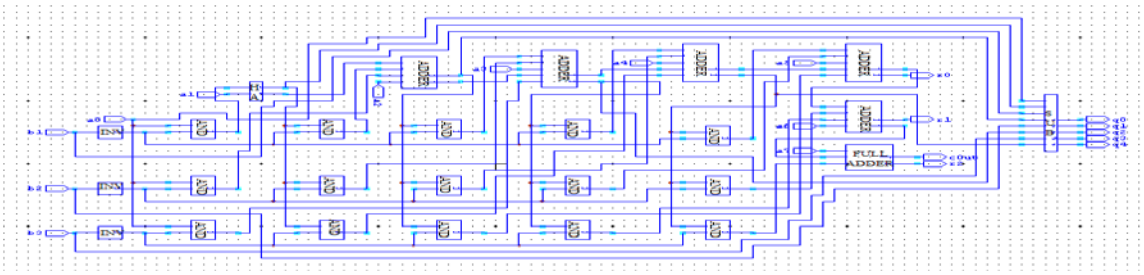

Fig.1. 8 by 4 bit Vedic divider

Q0=A0 (5)
Q1= (Q0*B1) +A1 (6)
Q2= (Q0*B2) + (Q1*B1) +A2+C1 (7)
Q3= (Q0*B3) + (Q1+B2) + (Q2*B1) +A3+C2 (8)
Q4= (Q1*B3) + (Q2*B2) + (Q3*B1) +A4+C3 (9)
R0= (Q2*B3) + (Q3*B2) + (Q4*B1) +A5+C4 (10)
R1= (Q3*B3) + (Q4*B2) +A6+C5 (11)
R2= (Q4*B3) +A7+C6 (12)
Q0Q1Q2Q3Q4 - B1B2B3=Q0Q1Q2Q3Q4 (Final quotient) (13)

4.2. 16 by 8 bit Vedic divider

The modified Vedic algorithm is elaborated using sixteen dividend data inputs and eight divisor data inputssee in table3.According to Paravartya sutra, all the divisor inputs are complemented except MSB bit.By successive addition of columns quotient and remainders are obtained.

Table 3. Vedic algorithm for 16 by 8 bit Division

Divisor	Dividend
1 0 1 1 0 0 1 1	1 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1
-1 0 0 -1 -1 0 0	-1 0 0 -1 -1 0 0
	-1 0 0 -1 -1 0 0
	0 0 0 0 0 0 0
	0 0 0 0 0 0 0

	0 0 0 0 0 0 0	
	-1 0 0 -1 -1 0 0	
	-1 0 0 -1 -1 0 0	
	0 0 0 0 0 0 0	
	0 0 0 0 0 0 0	
	1 1 0 0 0 -1 -1 0 0	1 1 1 1 0 1 1
	Q=110000000-0110011	R=1111011
	Q=110110011	

The modified Vedic divider hardware block consists A0A1A2A3A4A5A6A7A8A9A10A11A12A13A14A15as dividend digits and B0B1B2B3B4B5B6B7 as divisor digitssee in fig.2. In the first step, MSB bit A0 of dividend is partially multiplied with complemented divisor bits B1B2B3B4B5B6B7, multiplied data added with next dividend input A1. These addition results are partially multiplied with complemented divisor inputs and multiplied data again added with next dividend input A2.The each successive additionresult is used as one of the multiplicand for further partial multiplication. This cycle repeats again and again until addition of dividend A15 is carried out. In this operation, find two negative numberstake first complement on these numbers and then subtraction takes place.During operation, carries generates in a row propagate to next row and so on. The addition results are carried out through full and half adders while as AND operation is carried out through AND blocks. This design is implemented by observing the 8 by 4 bit Vedic divider. Reduce the operational blocks and fast in response are the important features of Vedic division than conventional techniques. Output results are consider in eq. (14) to eq.(30), quotient consider in eq. (14) to eq. (22) and remainder in eq. (23) to eq. (29). Final quotient consider in eq. (30).

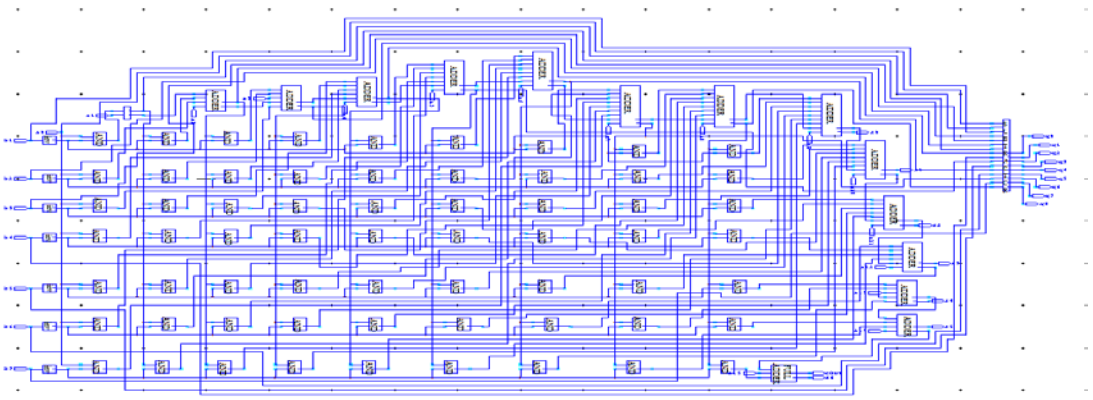

Fig.2. 16 by 8 bit Vedic divider

$$Q0=A0 \quad (14)$$

$$Q1= (Q0*B1) +A1 \quad (15)$$

$$Q2= (Q0*B2) + (Q1*B1) +A2+C1 \quad (16)$$

$$Q3= (Q0*B3) + (Q1*B2) + (Q2*B1) +A3+C2 \quad (17)$$

$$Q4= (Q0*B4) + (Q1*B3) + (Q2*B2) + (Q3*B1) +A4+C3 \quad (18)$$

$$Q5=(Q0*B5)+(Q1*B4)+(Q2*B3)+(Q3*B2)+(Q4*B1)+A5+C4 \quad (19)$$

$$Q6=(Q0*B6)+(Q1*B5)+(Q2*B4)+(Q3*B3)+(Q4*B2)+(Q5*B1)+A6+C5 \quad (20)$$

$$Q7=(Q0*B7)+(Q1*B6)+(Q2*B5)+(Q3*B4)+(Q4*B3)+(Q5*B2)+(Q6*B1)+A7+C6 \quad (21)$$

$$Q8=(Q1*B7)+(Q2*B6)+(Q3*B5)+(Q4*B4)+(Q5*B3)+(Q6*B2)+(Q7*B1)+A8+C7 \quad (22)$$

R0=(Q2*B7)+(Q3*B6)+(Q4*B5)+(Q5*B4)+(Q6*B3)+(Q7*B2)+(Q8*B1)+
A9+C8 (23)
R1=(Q3*B7)+(Q4*B6)+(Q5*B5)+(Q6*B4)+(Q7*B3)+(Q8*B2)+A10+C9 (24)
R2=(Q4*B7)+(Q5*B6)+(Q6*B5)+(Q7*B4)+(Q8*B3)+A11+C10 (25)
R3=(Q5*B7)+(Q6*B6)+(Q7*B5)+(Q8*B4)+A12+C11 (26)
R4=(Q6*B7)+(Q7*B6)+(Q8*B5)+A13+C12 (27)
R5=(Q7*B7)+(Q8*B6)+A14+C13 (28)
R6=(Q8*B7)+A15+C14 (29)
Q0Q1Q2Q3Q4Q5Q6Q7Q8 - B1B2B3B4B5B6B7
Q0Q1Q2Q3Q4Q5Q6Q7Q8 (Final quotient) (30)

5. Results And Discussion

5.1. 8 by 4 bit Vedic divider

The synthesis report of proposed division algorithm is shown in table 4. The total power dissipation in the Vedic divider is 12.75mw and it produces total propagation delay nearly to 5.83ns. The comparison result shows that proposed division method provides 70% less delay, 62% reduction intotal power and 88% less PDP as compared to previous work [8].

Table 4. Synthesis result comparison for 8 by 4 bit Vedic divider

Name	Average Power(mw)	Delay(ns)	PDP(pj)
8 by 4 previous work[8]	34	19.9	676.6
8 by 4 proposed work	12.75	5.83	74.33

The graphical representation of Average power, propagation delay and PDP for conventional and proposed work is illustrates in fig.3.

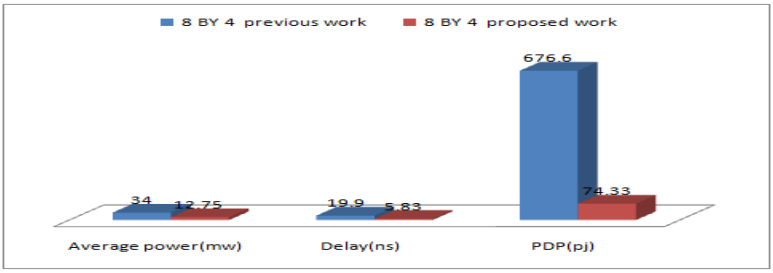

Fig.3. Average power, delay and PDP of 4 by 2 bit Vedic divider

From the synthesis report it is clear that proposed divider hardware consists less modules in comparison to conventional technique for the implementation of 8 by 4 bit divider as shown in table 5.

Table 5. Comparison of logic function used for 8 by 4 bit division

Logic cells	Previous work[8]	Proposed work

1 -bit adder carry out	6	3
2 -bit adder	6	-
2 -bit adder carry out	5	9
3- bit adder	4	-
3- bit adder carry out	4	-
5- bit adder	1	-
5 bitSubtractor	1	1
Comparators	11	-
Multiplexer	7	-
Xors	8	3
1 bit And logic	-	15
OR	-	5

5.2. 16 by 8 bit Vedic divider

The synthesis report of proposed 16 by 8 bit division algorithm is shown in table 6. The simulation results shows that Vedic divider using 13T full adder provides 13% delay reduction, 7% reduction in total power dissipation and 20% less PDP against 26T full adder.

Table 6. Comparison of result for 8 by 4 bit Vedic divider

Name	Average Power(mw)	Delay(ns)	PDP(pj)
16 by 8 using 26T FA	16.6	6.81	113.04
16 by 8 using 13T FA	15.39	5.90	90.8

The graphical representation of Average power, propagation delay and PDP using 13T and 26T full adder is illustrates in fig.4.

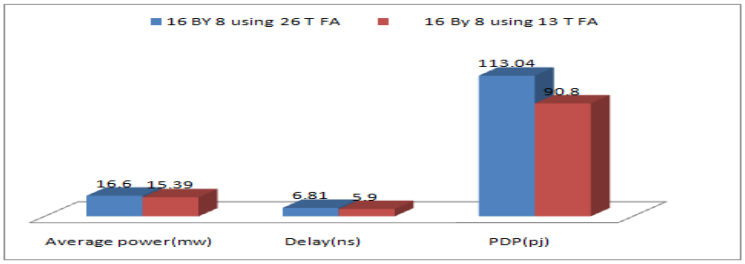

Fig.4. Average power, delay and PDP of 4 by 2 bit Vedic divider

6. Conclusion

The proposed Vedic divider is simulated on Tanner EDA 13.0 at 32nm technology file using 1.0v supply. The delay incurred by proposed 8 by 4 bit Vedic divider is 70% less than incurred in previous work. It is found that 62% power reduction by proposed work against previous work [5].All the simulation results are operated at 1 GHZ frequency. Obtained results facilitate the usage of proposed Vedic divider for high speed applications like radar technology and digital signal processing.
The future work extended the 16 by 8 bit Vedic divider upto32 by 16bit. In this paper, the proposed Vedic divider is implemented using binary format. Future work also extended on binary as well as on BCD format.

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References

[1] Siba Kumar Panda and AratiSahu, "A Novel Vedic Divider Architecture with Reduced Delay for VLSI Applications", I*nternational Journal of Computer Applications(IJCA)*, Vol.17, pp.31-36, 2015.

[2] RuchiAnchaliya, Chiranjeevi G.N. and Subhash Kulkarni, "Efficient Computing Techniques using Vedic Mathematics Sutras", I*nternational Journal Of Innovative Research In Electrical, Electronics, Instrumentation And Control Engineering(IJIREEICE),* Vol. 3, pp.24-27, 2015.

[3] DalalRutwikKishor andV.S.KanchanaBhaaskaran, "Low Power Divider Using Vedic Mathematics", *IEEE International Conference on Advances in Computing, Communications and Informatics,* pp.575-580, 2014.

[4] Miss. AditiS.Tadas andProf. Dinesh Rotake,"Design and Simulation of 64 Bit Divider Using Vedic Mathematics", *International journal of advanced information and communication technology (IJAICT)*, Vol.1, pp.608-609, 2014.

[5] Surabhi Jain, MukulPancholi, Harsh Garg and Sandeep Saini, "Binary Division Algorithm and High Speed Deconvolution Algorithm", *International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, pp.32-35, 2014.

[6] NajibGhatte, ShilpaPatil and Deepak Bhoir, "Single Precision Floating Point Division",*Proceedings of Fifth IRF International Conference,*pp.34-38, 2014.

[7] MansourehLabafniya and Mohammad Eshghi, "RNS Division Algorithm for 2^n-1 and 2^n Dividers", T*he 22nd Iranian Conference on Electrical Engineering (ICEE), IEEE,* pp.955-958, 2014.

[8] RatiranjanSenapati, Bandan Kumar Bhoi,Manoranjan Pradhan,"Novel Binary Divider Architecture for High Speed VLSI Applications",*Proceedings of IEEE conference on information and communication Technology,(2013),*pp.675-679, 2013.

[9] Greeshma Liz Jose andSani John,"VLSI Implementation Of Vedic Mathematics And Its Applications In RSA Cryptosystem", *International Journal of Innovative Research and Development*, Vol. 2,pp.297-303, 2013.

[10] Soma BhanuTej, "Vedic Divider - A High Performance computing Algorithm for VLSI Applications", *IEEE International Conference on Advances in Electronics, Computers and Communications*, pp.57–61, 2013.