Design of Power Aware 64 Bit Carry Select Adder for Low Power Arithmetic Circuits at 32nm Technology

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Abstract.As the technology is shrinking day by day, energy and leakage power becoming a critical parameter for modern VLSI designTo full fill the demand and challenge of customer industry is demanding circuits with low power and high performance. In this paper, we have designed 64-bit modified carry select adder by using 6T MUX, 3TAND,3T XOR and 5Thalf adder configurations which has better performance parameter as compared to the existing design in the literature. To evaluate the performance of modified architecture of carry select adder, extensive simulations are performed by using different bit pattern in T-spice. Resultshows that 16-bit carry select adder having improvement in delay upto 34% and average power improves upto 91% and power delay product 92%. The design is extended up to 64bit Carry Select Adder. Results show that by modified Carry select adderconsume lesser average power and power delay product.

Keywords:BEC, RCA, SQRT-CSA,MUX and Power aware.

1. Introduction

Low-power, area-efficient, and high-performance VLSI systems are increasingly used in portable and mobile devices, multi standard wireless receivers, and biomedical instrumentation. An adder is the main component of an arithmetic unit[1]. A complex digital signal processing (DSP) system involves several adders. An efficient adder design essentially improves the performance of a complex DSP system. A ripple carry adder (RCA) uses a simple design, but carry propagation delay (CPD) is the main concern in this adder[7].Ripple Carry Adder (RCA) shows the compact design but their computation time is longer, Carry look-ahead and carry select (CS) methods have been suggested to reduce the CPD of adders [8] but needed more number of MOS transistors which further increases leakage and average power dissipation.
But the carry select adder provides a compromise between the small areas and longer delay of RCA and large area with small delay of Carry select adder[9]. In the past different types of carry select adder design were proposed for instance using BEC, CBL and new CSA using logic formulation. Every circuit design has own merits and demerits. All the simulations in this paper are carried out by using 32nm technology obtained from PTM [10].

2. Related Work

The most of the previous carry select adder design (CSLA) uses binary to excess-1 converter (BEC) or square root circuit which had many redundant logic operations [1]. In this modified CSA adder all thereredundant logic operation are eliminated which was present in the previous carry select adder design. A theoretical

estimate results shows that SQRT-CSLA involves nearly 35% less area–delay–product (ADP) compare to BEC-based SQRT-CSLA, proposed adder design is best among the existing SQRT-CSLA designs, for different bit-widths such as 16 bit, 32 bit and 64 bit.The design presentedin [2] has used 250-nm CMOS technology, which is based on a combination of CPL and CS logic to obtain a fast and power/area efficient adder design. Linear CSA using modified CPL design has 18.83% less delay with an increase of 5.4% power and with slight increase in transistor count of l.77% when compared with the results of proposed SQRT CSA using modified CPL. But CPL has disadvantage of signal degradation at the output if the signal pass through long rail of series transistors which further reduces the noise margin. Another design presented in [3] had used D-latch instead of using RCA. In this design, power and delay is reduced to 10.8% and 4.6% for 8bit, 17.73% and 49.3% for 16bit, 20% and 44.5% for 32bit, 21.9% and 59.8% for 64bit when compared to the Regular Carry Select Adder (CSLA). Another design presented in [4] have used SHM (Special Hardware using Multiplexers) at the second level of second block in 16-bit SQRT CSLA, observed that area is reduced by 13.5% and power dissipation is reduced by 6.4%. This proposed logic is designed in transistor level using 0.12µm technology in the Micro wind tool. But in this design delay was increased as compared to existing carry select adder design. The design presented in [5] a simple and efficient transistor-level modification in BEC-1 converter to reduce the area and power of the CSLA. Result shows that the modified BEC-MUX has a slightly larger delay (only 31.06%), but the power of the modified BEC-MUX are significantly reduced by 14.70%. in this leakage power and power delay product is not calculated.

In the paper [6] conventional CSLA is compared with Modified Carry select adder (MCSLA), Regular Square Root CSLA (SQRT CSLA), Modified SQRT CSLA and Proposed SQRT CSLA in terms of area, delay and average power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA.

3. Adder Design

Fig.1 shows the 2-bit CSA divide in different units like half sum generation unit (HSG),second part when carry 0 ,third part for carry 1, fourth unit for carry selection unit means MUX and last sum generation unit . All units explain in below diagram.

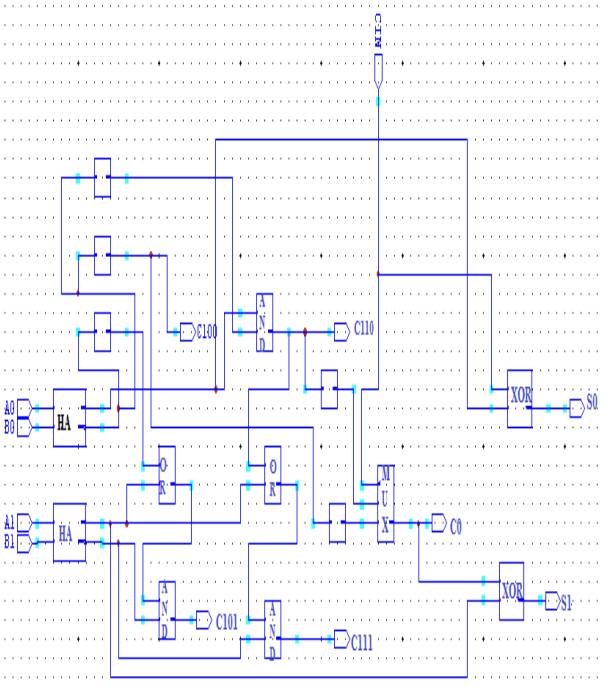


Fig. 1. 2 Bit Carry select adder

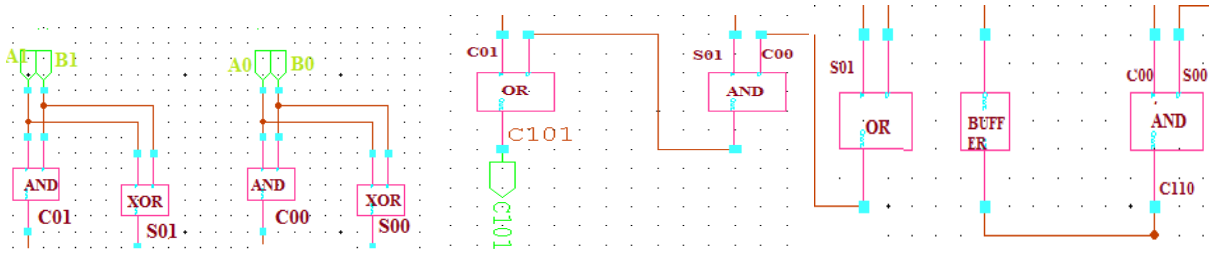
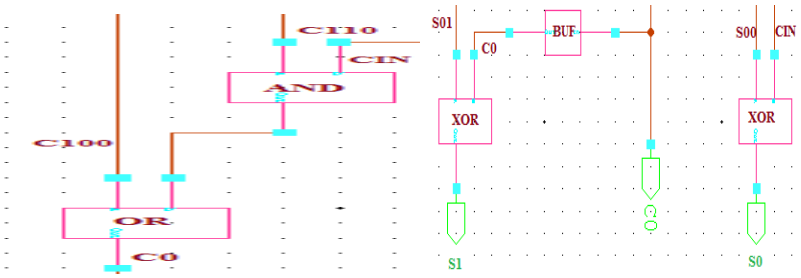


Fig.2(a) HSG unit**Fig. 2**(b) CG0 unit**Fig.2**(c) CG1 Unit



(d) (e)

Fig.2(d) Carry select unit**Fig.2**(e) Final sum generation

The power consumption of a CMOS transistor can be divided into three different components: dynamic, static (or leakage) and short circuit power consumption [1]. Dynamic and short circuit power are also collectively known as switching power, and are consumed when transistors change their logic state, but leakage power is consumed merely because the circuit is "powered-on". Switching power is consumed when signals through CMOS circuits change their logic state, resulting in the charging and discharging of load capacitors. Leakage Power is primarily due to the sub-threshold currents and reverse biased diodes in a CMOS transistor. Mathematically total power dissipation is given as:

$$P_{total} = P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

$$P_{total} = V^2_{dd}.f_{clk}.C_L.\alpha + \alpha/12\ (V_{dd} - 2V_{th})^3 t_r/t_f + I_{leakage} V_{dd}$$

Where f_{clk} is the system clock frequency, C_L is the load capacitance, α is the switching activity factor, $t_{r/}$, t_f is the rise and fall time of input signal, $I_{leakage}$is the total leakage current flowing through the device and Vdd is the supply voltage.

4. Proposed Adder

PProposed carry select adder design consist various units like half sum generation unit (HSG), second part when carry 0, third part for carry 1, fourth unit for carry selection unit means mux and last sum generation unit which is shown in Fig 3.2.

1) Half sum generation unit replaced with 5T half adder in place of AND and OR gates. Similar done with 16 bit, 32 bit and 64 bit architectures.
2) Carry selection unit when CIN is 0 select the first stage for carry and when cin =1 then select the second stage. In this we used simple 6T MUX architecture instead of gates.
3) At last sum generation unit replaced with 3T XOR configuration and also used 3T AND gate in place of AND gate.

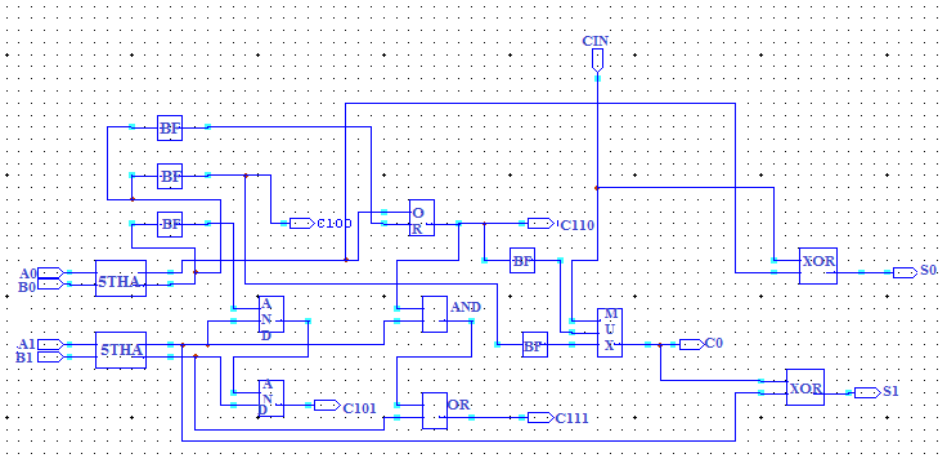


Fig. 3.2 bit modified CSA design

Due to the above mention modifications proposed design has lesser number of transistors as compared to existing adder design in the literature.

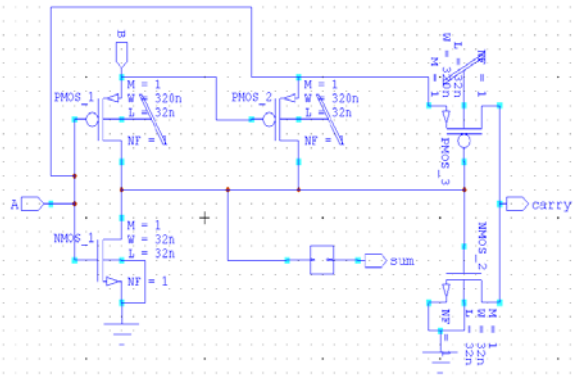


Fig. 4. 5T half adder design

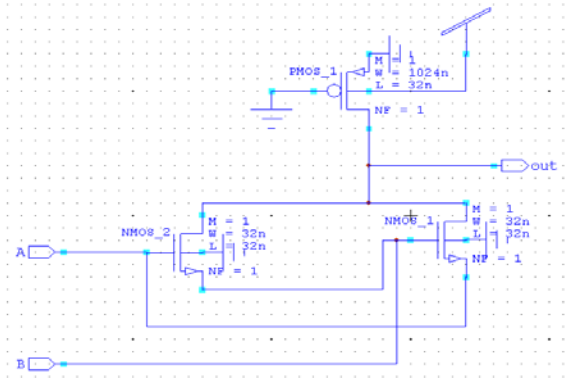


Fig. 5. 3T AND gate configuration

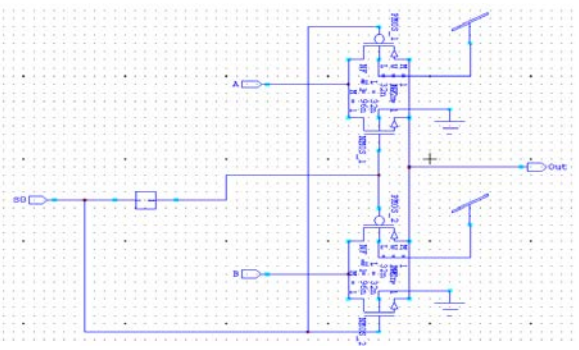


Fig. 6. 4T MUX circuit

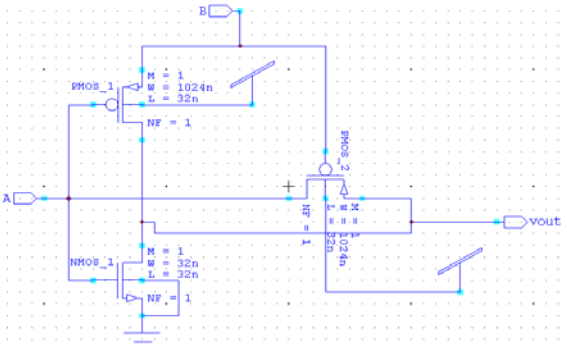


Fig. 7. 3T XOR configuration

Using 2 bit modified CSA we have designed 16-bit, 32-bit and 64-bit. And also we have proposed new architecture of CSA, in this architecture we have designed 16 bit, 32 and 64 bit CSA by using symmetrical blocks of 2*2 modified CSA.16 bit shown below same as we have designed 32 bit and 64 bit.

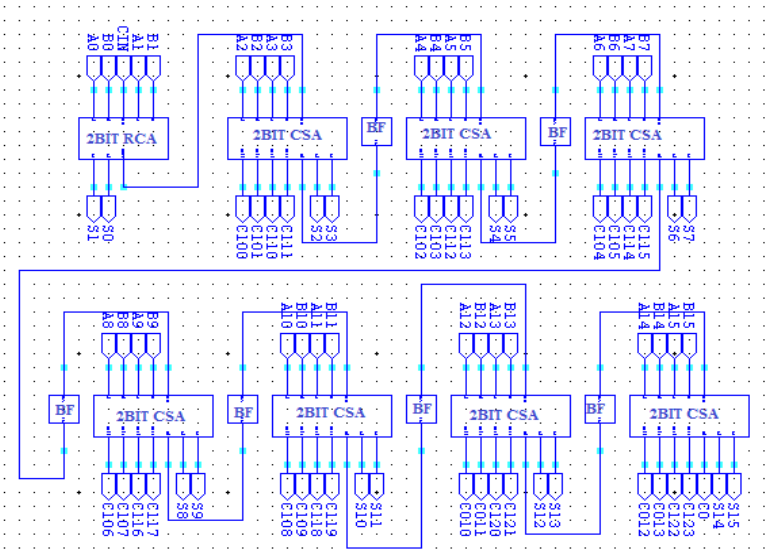


Fig. 8. 16 bit CSA by using modified CSA Blocks

5. Simulated Results

In this architecture we have designed 16 bit, 32bit and 64 bit CSA using modified CSA design and calculate all parameter like average power,delay,leakage power and power delay product for better result comparison. All the results and simulation are done on TANNER EDA Tool 13.0 at 1GHz frequency with 1.0 v supply voltage. All designed used different gate width of 32nm for NMOS and PMOS transistor.

Table 1. Result of proposed design at different bit-width with 1Ghz frequency

Width	Average power (mW)	Delay(ns)	PDP(pj)	Leakage(mW)
16bit	0.259	0.843	0.2183	0.0721
32bit	0.5359	1.6129	0.8643	0.125
64bit	0.1588	3.1725	0.5025	0.2365

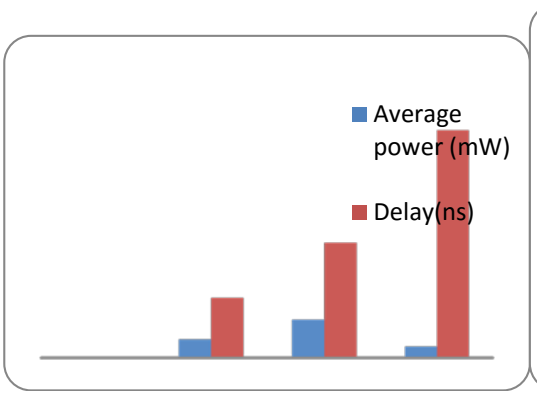


Fig. 9. Comparison of average power and delay

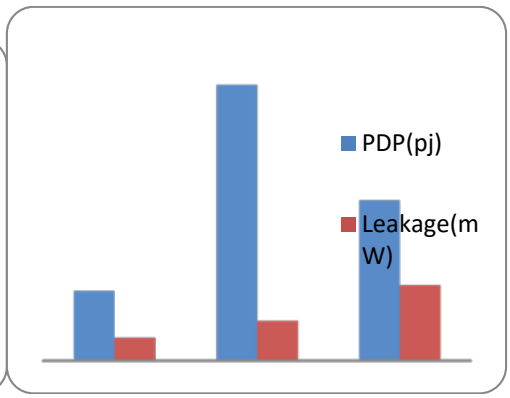
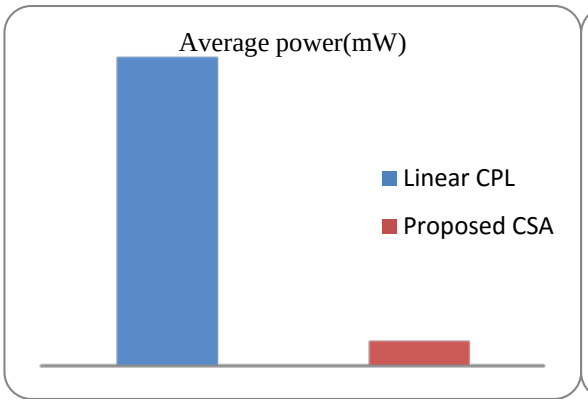


Fig. 10. PDP and leakage power dissipation

Because base paper results was evaluated on 100Mhz so we have also characterise our circuit at 100Mhz frequency and compare the result a shown in Table 2.

Table 2.16 bit CSA result comparison at 100MHZ

Type of adder	Average power(mW)	Delay (ns)	PDP(pj)
Linear CPL	5.698	1.25	7.12
Proposed CSA	0.4591	0.81706	0.3751
Linear CPL	5.698	1.25	7.12



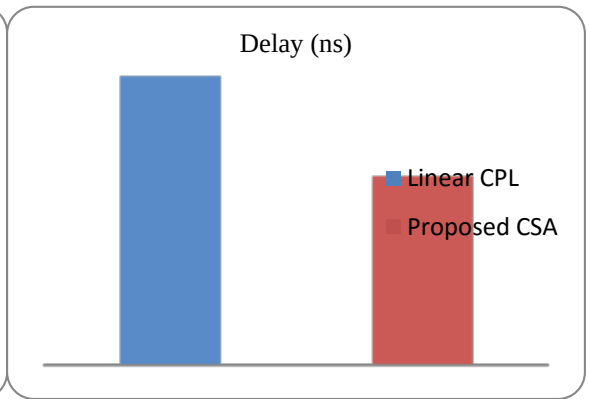


Fig. 11. Average power comparison**Fig. 12.** Delay comparison

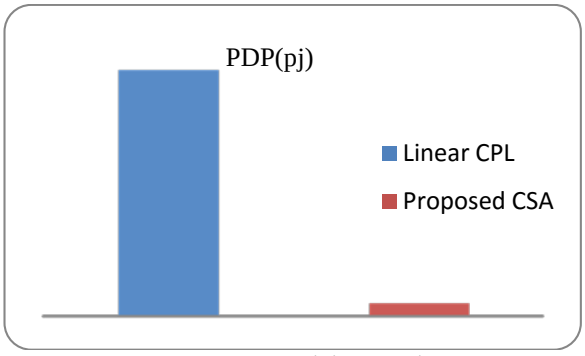


Fig. 13. Power delay product

6. Conclusion

In paper we have designed modified architecture of CSA by using 2*2 symmetrical blocks of modified CSA.Result shows that modified carry select adder design has lesser average power, delay, leakage power and power delay product. Modified CSA consumed 0.4591mW power, 0.3751pj PDP and having delay of 0.81706ns .Results shows that modified CSA is having 34% lesser delay as compared to existing CPL design at 1.0 supply voltage. Due to these modifications, proposed power aware carry select adder has wide scope for low power arithmetic circuits.

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