

# Design of Low Power and area efficient Sqrt Carry Select Adder using Parallel Prefix Adder Structure

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**Abstract.** The Sqrt Carry Select Adder (CSA) architectures using parallel prefix adder instead of Ripple Carry Adders (RCA) are implemented and analyzed in this paper. Brent Kung (BK) parallel prefix structure uses to designed a Square Root Carry-Select Adder (Sqrt CSA) at different word size and reduced area and power dissipation as compared to that of conventional Sqrt CSA. Ripple Carry Adder (RCA) takes longer computation time and Carry Look-ahead scheme (CLA) used to derive fast results but they increase in area and, the carry complexity increases by increasing the width of the adder for the higher bit. Carry Select Adder is a best compromise between RCA and CLA in term of area and delay. The architecture of 16-bit BK Sqrt CSA is configured into five different stages and it extends up to 32-bit. Power, delay, PDP and Transistor count of 16 bit adder architectures are calculated at different stage level at 1.0v input voltage. The architecture has been synthesized at 32nm technology at 1.0v using Tanner EDA tool 13.0v. The simulations of Modified Sqrt BKA CSA are performed in T-Spice. The results depict that Modified BKA Sqrt CSA is better than all the other adder architectures in terms of power, delay and area.

**Keywords:** Parallel Prefix Adder(PPA), Modified Square Root Brent Kung Adder Carry Select adder (Sqrt BKA CSA), Binary-to-excess-1 converter (BEC), etc.

## 1. Introduction

VLSI integer Adders and multipliers are important elements in general purpose and digital-signal processing processors since they are employed in the design of Arithmetic-Logic Units, in address generation units and in floating-point arithmetic data paths [1]. Adders are used not only in the Arithmetic logic units, but also in other parts of the processor. They are also responsible for minimum clock cycle time in digital systems. The propagation delay of an adder unit puts a major constraint on the minimum cycle time or maximum clock frequency. For adding binary numbers several adder structures based on different design ideas has been proposed to reduce the power consumption, delay and high speed. These adders are like Ripple carry adder (RCA), Carry Look Ahead adder (CLA) and carry select adder (CSA). Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a best compromise between RCA and CLA in term of area and delay [2]. The parallel Prefix Adders (PPAs) are the target of most recent scientific investigations. PPAs have unified organizations in their structure and are superior over the other adder structures. They are in different structures, but most of their differences belong to their propagate tree structure [3].

Conventional Carry Select Adder is designed using Ripple Carry Adders (RCAs), Binary to Excess-1 converter (BEC) circuit and then there is a multiplexer stage. In this paper, The modified Sqrt CSLA is realized by replacing Ripple carry adder with Brent Kung adder and the BEC block has been modified by using Half adder instead of XOR AND combination in ordinary BEC circuit. Because delay and power



consumption of RCA is large. Therefore, we have replaced it with parallel prefix structure which gives power and area efficient Sqrt BKA CSA.

The paper is organized as follows: discussion about previous work in section 2. In Section 3, parallel prefix adders are illustrated. Section 4 explains Design methodology. In section 5 Simulation results and compare of the architectures of Modified Sqrt conventional Sqrt based on different parameters for different stages and section 6 Concludes and Future work.

## 2. Related Work

This evaluated the Sqrt CSA was an architecture level modification to reduce area and power dissipation as compared to that of conventional CSA. Conventional CSA with  $C_{in}=1$  block was replaced with binary-to-excess-1 converter (BEC) in the modified Sqrt CSA structure. The average power, delay, Transistor Count were found to be 285.6  $\mu$ W, 4.382ns, 196 respectively, and hence the PDP of the adder was 1251.49pJ [4]. This design [9] described a simple and efficient transistor level modification in BEC-1 converter to significantly reduce the area and power of the CSLA. Based on this modification 16-b square-root CSLA (Sqrt CSLA) architecture have been developed and compared with the Sqrt CSLA architecture using ordinary BEC-1 converter. The results analysis shows that the proposed CSLA structure is better than the Sqrt CSLA with ordinary BEC-1 converter. The adder design evaluated the carry select (CS) operation was scheduled before the calculation of final-sum, which were different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to  $c_{in} = 0$  and 1) and fixed  $c_{in}$  bits are used for logic optimization of CS and generation units. The proposed BEC-based CSLA design involves 48% more ADP and consumes 50% more energy than the proposed Sqrt-CSLA, on average, for different bit-widths [6].

## 3. Parallel Prefix Adder

Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. PPA is a two step process to generate the carry [11]. Parallel-prefix structures are found to be common in high performance adders because of the delay is logarithmically proportional to the adder width and these are faster adders and used for high performance arithmetic structures in industries. They are in different structures, but most of their differences belong to their propagate tree structure. The parallel prefix addition basically consists of 3 stages.

- Pre computation
- Prefix stage
- Post processing computation

### 3.1. Pre-processing stage

In this stage we compute, generate and propagate signals are used to generate carry input of each adder. A and B are the inputs. These signals are given by the equation 1 & 2.

$$P_i = A_i \text{ xor } B_i \tag{1}$$

$$G_i = A_i \text{ and } B_i \tag{2}$$

### 3.2. Carry generation network (Prefix stage)

In the prefix stage, we compute carries equivalent to each bit. This operation provided carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. Group carry propagate and generate signals are used as intermediate signals and are computed at each bit. The black cell (BC) generates pair of propagate and generate signal, the gray cell (GC) generate only left generate signal. Which are given by the logic equations 3, 5&7.

$$CP_{i,j} = P_{i:k+1} \cdot P_{k:j} \tag{3}$$

$$CP_0 = P_1 \cdot P_j \tag{4}$$



$$CG_{i,j} = G_{i:k+1} + (P_{i:k+1} \cdot G_{k;j}) \tag{5}$$

$$CG_0 = P_1 \cdot G_1 \tag{6}$$

$$C_{i-1} = (P_i + C_i) \cdot G_i \tag{7}$$

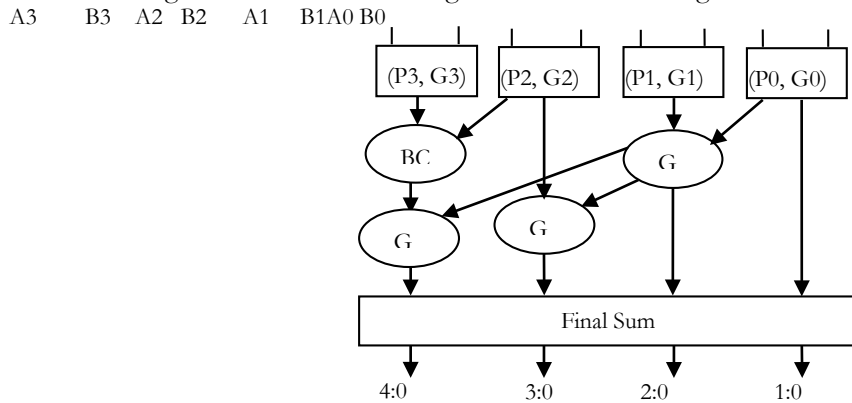
**3.3. Post processing Stage**

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 8.

$$\oplus S_i = P_i \ C_{i-1} \tag{8}$$

**3.4. Brent-Kung Adder**

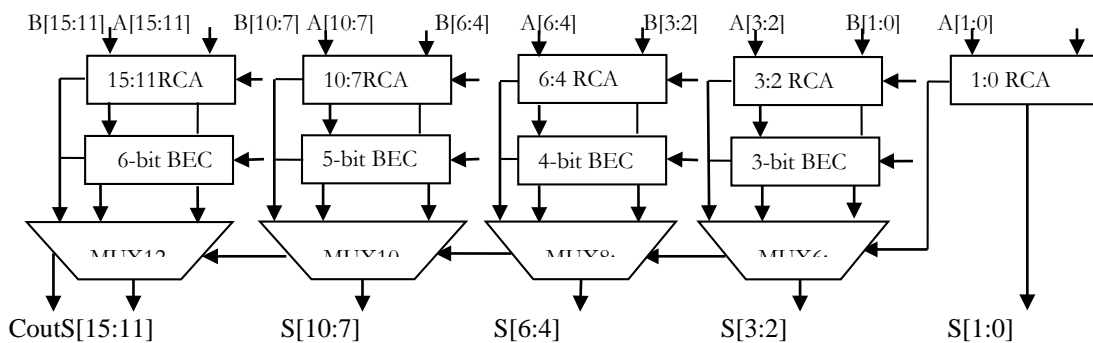
The Brent-Kung (BK) adder in 1982 was proposed to resolve the drawbacks in KS adder. It is one of the parallel prefix adders. Brent-Kung adder is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages [1]. Brent-Kung approach focused on optimal area design issue to have the minimal number of nodes at the cost of maximum logic depth. But the gate level depth of Brent-Kung adders is 0, so the speed is lower [7]. The block diagram of 4-bit Brent-Kung adder is shown in Fig. 1.



**Fig. 1.** Block diagram of 4-bit Brent Kung adder

**3.5. 16-bit CONVENTIONAL SQRT CSA**

The block diagram of architecture of conventional 16-bit SQRT CSA is shown in fig.2. It has been designed using five different stages. Each stage contains one RCA, BEC and then MUX.



**Fig. 2.** Block diagram of architecture of conventional 16-bit SQRT CSA

The first stage consists of only 2-bit RCA. This RCA designed using simply two cascaded 1-bit full adder circuit. It is the rest stage of CSA based circuit. The CMOS transistor requirement for stage-2 of conventional 16-bit SQRT CSA is given below.



It consists of one full adder, one half adder for 3:2 RCA, 3-bit BEC and 6:3 MUX stage.

Transistor count = 74 (FA + HA + 3-bit BEC + 6:3 MUX)

FA = 20 (1 x 20), HA = 12 (1 x 12)

3-bit = 24 (AND = 6, NOT = 2, XOR = 16), 6:3 MUX = 18 (3 x 6)

## 4. Design Methodology

### 4.1. Modified 4-bit Binary-to-Excess-1

A different add-one scheme like Binary to Excess-1 Converter (BEC) is used to add 1 to the input numbers. BEC has less area of circuit because less number of logic gates is required for implementation. So, RCA replaced by BEC in SQRT CSA. The circuit of BEC is modified using Half Adder instead of using XOR, AND Gate in Ordinary BEC. The circuit of Modified 4-bit BEC is designed and modified using Three HA, one XOR and 1 INVERTER as shown in Fig.3.

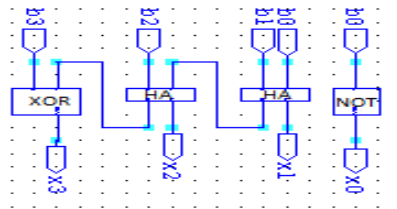
The Boolean expressions of 4-bit BEC are listed below:-

$$X_0 = \text{NOT } B_0$$

$$X_1 = B_0 \text{ XOR } B_1$$

$$X_2 = B_2 \text{ XOR } (B_0 \text{ AND } B_1)$$

$$X_3 = B_3 \text{ XOR } (B_0 \text{ AND } B_1 \text{ AND } B_2)$$



**Fig. 3.** Circuit Diagram of Binary-to-Excess-1 Converter

### 4.2. AREA EVALUATION OF 16-BIT SQRT BKA CSA

The Schematic diagram of architecture of 16-bit SQRT BKA CSA is shown in Fig. 10. This architecture is configured with five different stages. Each stage consist single Brent Kung Adder, modified Binary to Excess 1 Converter and then multiplexer stage. The RCA block in ordinary SQRT CSA is replaced with Parallel prefix adder i.e. Brent Kung adder.

The first stage of 16 bit architecture is simply a 2-bit Parallel Prefix Brent Kung Adder circuit. We know that the Parallel Prefix Adder consists of Pre-processing, Prefix and Post-processing Circuit.

The Second stage of 16 bit architecture is consists of 2 bit BKA, 3-bit BEC and 6:3 MUX as shown in Fig. 9. The MOS transistor requirements for stage-2 in modified 16-bit SQRT CSA are given below:

2-bit BKA = Pre-process + Prefix + Post process = 10 + 20 + 8 = 38, 3-bit BEC=11 (XOR=4, NOT=2, HA=5)

6:3 MUX= 18 (3x6), So, Total transistor count of stage-2 = 67 (2-bit BKA+3-bit BEC+ MUX 6:3) = 38 + 11 + 18 = 67.

Similarly, all the other group gate requirements are calculated and listed as shown in Table 1.

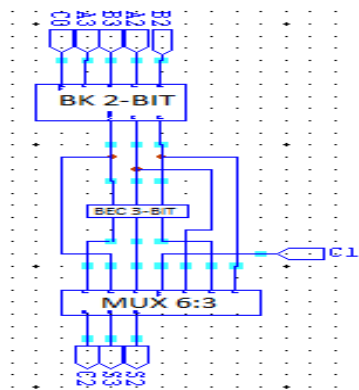


Fig. 4. Circuit Diagram of Stage-2

Table 1. Parameters of 16-bit SQRT BKA CSA.

Stage No. (No. of Bits)	Transistor Count	Power ( $\mu$ W)	Delay (ns)	PDP (fj)
Stage 1 (2 bit)	38	8.80	0.226	1.988
Stage 2 (2 bit)	67	11.92	0.580	6.913
Stage 3 (3 bit)	99	32.21	0.735	23.674
Stage 4 (4 bit)	149	37.06	1.343	49.771
Stage 5 (5 bit)	181	45.91	1.458	66.936
Total	534	135.90	4.342	149 .282

The architecture of modified 16-bit SQRT BKA CSA has 5 stages of different size Brent Kung adder as shown in fig. 5. Each stage involves single BK, Modified BEC and multiplexer. For N-bit BKA, N+1 BEC is required. The schematic of 16-bit SQRT BKA CSA is shown in Fig. The parameters such as power consumption, Delay, transistor count and PDP of this adder are calculated for 16-bit and 32-bit word size.

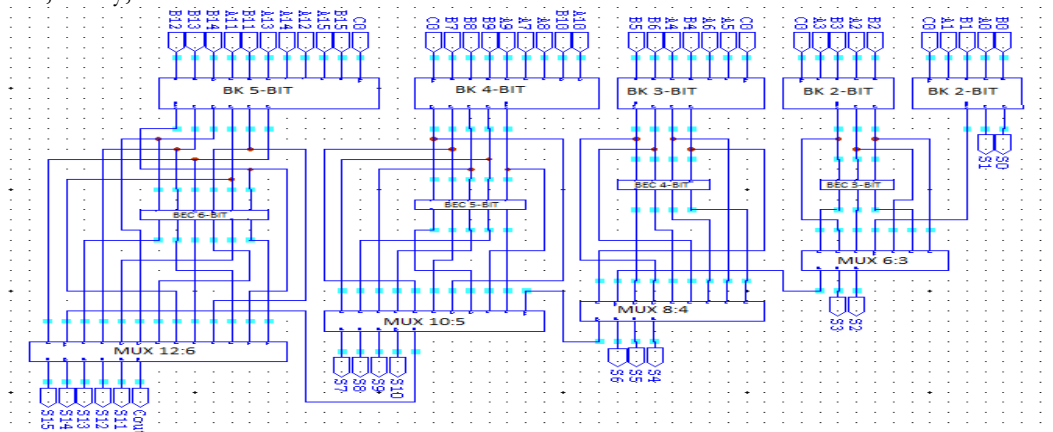


Fig.5. Schematic diagram of 16-bit SQRT BKA CSA

## 5. Results and Simulations

The Modified SQRT BKA CSA is designed in Tanner EDA 13.0 version tool using 32nm CMOS technology. The Simulations of architecture are performed using T-SPIICE and supply voltage of 1.0V. The waveforms are obtained using W-Edit. The comparison for different parameters like power, delay, PDP and Transistor

count for different stages of modified SQR T BKA CSA with Conventional SQR T CSA for 16-bit word size is shown in Table 2.

**Table 2.** Comparison of Modified 16-bit SQR T BKA CSA with Conventional SQR T CSA.

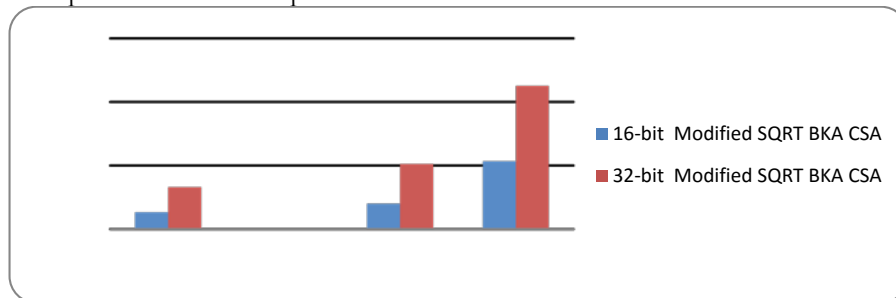
Stage No.	SQR T CSA	Delay (ns)	Power (μW)	PDP (fj)	Transistor Count
Stage 1	Conventional	1.619	84.2	136.31	40
	Modified	0.226	8.80	1.988	38
Stage 2	Conventional	1.858	108.5	201.59	74
	Modified	0.580	11.92	6.913	67
Stage 3	Conventional	2.302	153.9	354.27	116
	Modified	0.735	32.21	23.674	99
Stage 4	Conventional	3.432	206.1	707.33	156
	Modified	1.343	37.06	49.771	149
Stage 5	Conventional	4.082	285.6	1251.49	196
	Modified	1.458	45.91	66.936	181

The analysis results concluded that Modified SQR T BKA CSA shows better results as compared to Conventional SQR T CSA and all other Adder in terms of all parameters like power, delay and area. The parameters like Power consumption, Delay, Power delay product (PDP), and Transistor count of proposed SQR T CSA has been calculated for 16-bit and 32-bit word size as listed in Table 3.

**Table 3.** Parameters of Modified 16-bit and 32-bit SQR T CSA.

Word Size	Transistor Count	Power (μW)	Delay (ns)	PDP (fj)
16-bit	534	133.08	1.51	200.95
32-bit	1127	330.92	1.55	512.92

The graphical representation for all parameters of 16-bit and 32-bit word size is shown in Fig. 6.



**Fig. 6.** Graphical representations for all parameters of 16 bit and 32 bit SQR T BKA CSA

## 6. Conclusion

In this work, A Square Root Carry Select Adder using Parallel Prefix Adder is proposed which is designed using Parallel prefix adder i.e., Brent Kung Adder and Modified Binary to Excess-1 Converter instead of using Ripple Carry Adder in order to reduce area, delay and power consumption of an adder architecture. Here,



the architecture of SQRT BKA CSA adder is designed for 16-Bit and 32-Bit word size. As, parallel prefix adders derive fast results therefore, Brent Kung adder is used. The calculated results conclude that Square Root Carry Select Adder using Brent Kung Parallel prefix adder is better in terms of power consumption, Delay and PDP when compared with other adder. The Area of adder is also reduced by reducing Transistor count and it can be used in different applications of adders. This work can be extended for higher number of bit word sizes also. These parallel prefix structures can be replaced with other parallel Prefix structures.

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