# High Speed 16- Bit Vedic Multiplier Using Modified Carry Select Adder

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**Abstract.** In this paper, a low power and high speed 16x16 Vedic Multiplier is designed using modified carry select adder. Modified Carry Select Adder employs a multiplexer and XOR gate based circuit on the intermediate stages instead of BEC and multiplexer which gives low power and high speed of operation. Vedic multiplier is based on the sutra "Urdhva-Tiryakbhyam" (Vertically and crosswise). It is one of the sutras of Vedic mathematics for multiplication. This sutra used both for decimal multiplication and binary multiplication. In this paper, the main goal is to optimize power and speed of multiplier. Simulation result shows that the proposed architecture achieves advantages in terms of PDP (Power delay product) and latency. The latency count improves as compared to the Dadda multiplier. All the Simulations are carried out in H-Spice at 32nm process technology.

**Keywords:**Carry Select Adder, Vedic Multiplier, Ripple Carry Adder, Binary to Excess Converter, Urdhva-Tiryakbhyam.

## 1. Introduction

A multiplier is one of the key hardware blocks in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. Vedic mathematics is used to reduce the computational time as compared to classical method and hence requires less hardware for when implemented on silicon. There are two constraints in multiplier which limit the speed: latency and throughput. Latency is real delay of computing a function, a measure of how long after the inputs to the device is stable, is the final result available on the outputs. Throughput is a measure of how many multiplications can be performed in a given amount of time. The Word "Vedic"is derived from the "Veda" which means the "store-house of all knowledge" [3]. Vedic mathematics is based on sixteen sutras that are related to the different branches of mathematics like algebra, arithmetic geometry [5]. Array multiplier reduces delay, but it requires a large numbers of gates [7]. Booth multipliers are used for signed binary numbers, but it does not work when there are alternate zeros and ones [6]. Wallace Tree multiplier works at high speed, exhibits structural irregularity, but having more complex hardware [12]. Braun multiplier is one of which require $n^2$ gates and (n-1) no. of adder which in turn increase the complexity and area of design [1] [5]. Dadda Tree multiplier work at high speed, but exhibits much higher circuit complexity [2] [3].

## 2. Related Work

In [2] author presented the comparison of the VLSI design of uniform carry select adder (UCSLA)-based multiplier technique. Area and power reduced in UCSLA- multiplier technique. Result shows that timing delay was reduced by 11.11 % by the UCSLA-based multiplier. Simulation results were carried out with TSMC 45 nm technology. Latency is not measured in UCSLA-based multiplier.

In [4] Multiplier design based on ancient Indian Vedic multiplication process and the low power energy recovery (DCPAL) was presented. Simulations were performed at 25 MHz frequency and simulated at 45nm technology. Latency and Leakage power is not measured in DCPAL based multiplier.

In [6] author presented the design of Multiplier based on Vedic multiplication sutra "Urdhva Tiryakbhyam". Simulation results were carried out in T- Spice in 45nm Technology. Leakage power is not optimize in this paper.

Compressor based Vedic multiplier with Urdhva Tiryakbhyam sutra has been reported in [8]. It shows considerable improvements in speed and area efficiency over the conventional ones. Result shows that an improvement of 3% over the Modified Booth algorithm was observed. Latency is not measured in Compressor based multiplier.

In [9] Dada tree multiplier was simulated to reduce the partial product by using the Sklansky tree adder in the final stage output instead of ripple carry adder. The latency count was reduced using Sklansky tree adder. Result shows that speed of Dadda multiplier was increased by 33.3% than the conventional Wallace tree multiplier. Delay and Leakage power is not optimize in this paper.

Vedic multiplier using 2N-2P type of charge recovery logic structure was implemented in [10]. Simulation result shows reduction in average power consumption by 77.66%. Delay, Latency and Leakage power is not characterised in this design.

## 3. Vedic Mathematical Algorithms

The Vedic mathematics reduces the complex calculations into simpler by applying 16 sutras. These Vedic mathematic techniques are very efficient for multiplication. Here "Urdhva-Tiryakbhyam" sutra applied for multiplication is discussed as below:

### 3.1. Urdhva-Tiryakbhyam Sutra (Vertically and Crosswise)

In this section we propose a Vedic multiplication technique which is based on "Urdhva-Tiryakbhyam – Vertically and crosswise" sutra. Vedic multiplier technique consists of generation of parallel partial products and addition operation simultaneously [3] [11].This algorithm can be used for 2×2, 4×4, 8×8, 16×6....N×N bit multiplications. In this method sum and their partial products are calculated in parallel hence Vedic multiplier does not depend upon the processor clock frequency and reduces the power dissipation [5]. The use of "Urdhva-Tiryakbhyam sutra" for multiplication operation reduces the latency of a multiplier unit by introducing concurrent computing of partial products. The main advantage of the Vedic multiplier is that it reduces delay as well as power when compared with the exiting multipliers. To illustrate this technique, let us consider two decimal numbers 525 and 786 and Steps of multiplication are shown in Fig. 1.

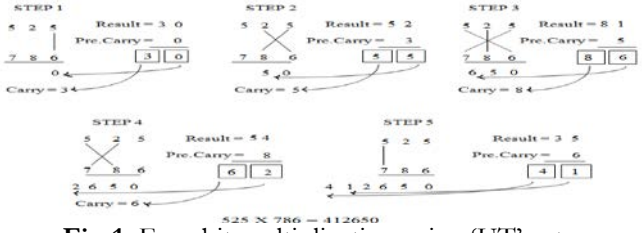


**Fig.1.** Four bit multiplication using 'UT' sutra

S0 is obtained by multiply the least significant bits of the multiplicand and multiplier. Numbers on both sides of the line are multiplied and added with carry from previous step in the last case. This generates one of the bits of the result sum and a carry. This carry is added in the next step hence the process goes on.

## 4. Modified Vedic Multiplier Architecture

### 4.1 2×2 Vedic Multiplier

The 2×2 Vedic Multiplier has been designed using two 5T half adder and four 3T AND gates as shown in Fig. 2. AND gates are used for partial product generation and half adders are used to realize the required addition process. In 2×2 Vedic multiplier, S0 is obtained by vertical multiplication of data bits A0 and B0, S1 is obtained by addition of crosswise bit product i.e. A1B0 and A0B1 and next S2 is obtained by adding the product vertical data bits A1 and B1 with the carry generated from the previous addition during S1. C2 is the nothing but carry generated in calculation of S (sum).

$$S0 = A0*B0 \quad (1)$$

$$C1S1 = (A1*B0) + (A0*B1) \quad (2)$$

$$C2S2 = (A1*B1) + C1 \quad (3)$$

Final result of above equations is C2S2S1S0.

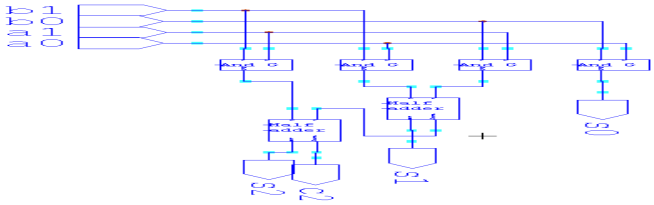

**Fig. 2.** Block Diagram of 2×2 Vedic Multiplier

### 4.2 4×4 Vedic Multiplier

The 4x4 Vedic Multiplier architecture is designed using four 2×2 Vedic Multiplier blocks and three 4-bit Ripple carry adder as shown in Fig.3 In the 4×4 Vedic Multiplier two four bit numbers are A and B such that the individual bits can be represented as the A3A2A1A0 and B3B2B1B0 are multiplied. In the 4×4 Vedic Multiplier partial product generation and additions are done concurrently.

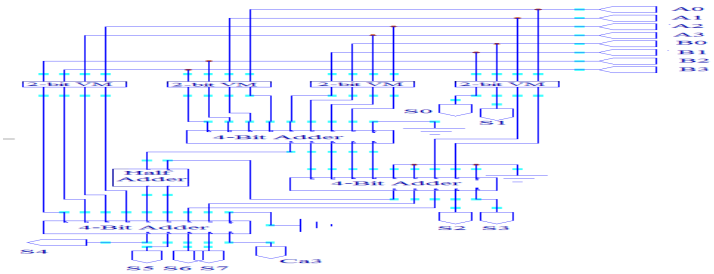

**Fig. 3.** Block Diagram of 4×4 Vedic Multiplier

The equations for 4×4 Vedic Multiplier are:

$$S0 = A0 * B0 \quad (4)$$

$$C1S1 = (A1 * B0) + (A0 * B1) \quad (5)$$

$$C2S2 = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 \quad (6)$$

$$C3S3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) + C2 \quad (7)$$

$$C4S4 = (A2 * B2) + (A3 * B1) + (A1 * B3) + C3 \quad (8)$$

$$C5S5 = (A3 * B2) + (A2 * B3) + C4 \quad (9)$$

$$C6S6 = (A3 * B3) + C5 \quad (10)$$

The final result is given as C6S6S5S4S3S2S1S0.

The Least Significant Bit (LSB) S0 is obtained easily by multiplying the LSBs of the multiplier and the multiplicand. After performing all the steps the result sum and Carry is obtained and in the same way at each step the previous stage carry is forwarded to the next stage and the process goes on. The final result is obtained by adding the outputs of 2×2 bit multipliers in a specific way. So we require three ripple carry adders at final stage as shown in Fig. 3.

### 4.3 8×8 Vedic Multiplier

The 8×8 Vedic Multiplier architecture is designed using four 4x4 Vedic Multiplier blocks and three 8-bit Modified Carry Select adder as shown in Fig.4.

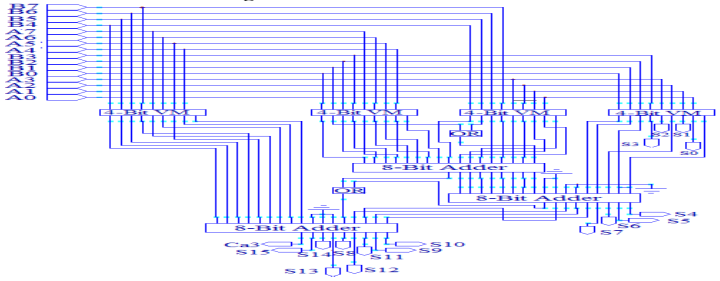


**Fig. 4.** Block Diagram of 8×8 Vedic Multiplier

In the 8×8 Vedic Multiplier two eight bit numbers A and B can be represented as the A7A6A5A4A3A2A1A0 and B7B6B5B4B3B2B1B0 are multiplied. The partial products are calculated in concurrent and hence delay obtained is decreased enormously for the increase in the number of bits. The Least Significant Bit (LSB) S0 is obtained easily by multiplying the LSBs of the multiplier and the multiplicand. After performing all the steps the result sum and carry is obtained and carry is propagate in the same way in the 4×4 bit Vedic multiplier. S15 to S0 are obtained upon application of the Urdhva Tiryakbhyam method of multiplication. The final result of 8x8 Vedic Multiplier is given as C16S15S14S13S12S11S10S9S8S7S6S5S4S3S2S1S0.

### 4.4 16×16 Vedic Multiplier

In this design two 8 bit numbers are A and B such that the individual bits can be represented as the A[15:0] and B[15:0].The procedure for multiplication Shown in the circuit diagram of 16×16 bit Vedic multiplier in Fig. 5. The final output can be obtained as the C16S[31:0]. S0 is obtained easily by multiplying the LSBs of the multiplier and the multiplicand. After performing all the steps the result and carry is obtained and carry is propagate in the same way as in the 8×8 bit Vedic multiplier.

16 Bit Modified Carry Select Adder: The Block diagram of the proposed Architecture consists of following parts

1) Ripple carry adder
2) Basic Unit (Multiplexer and XOR gate)

1) Ripple Carry Adder: Ripple carry adder is designed using 13T full adders for the addition of 8-bit numbers. A 2-bit RCA contain one 13T full adder and one 5T half Adder and same process for 3-bit, 4-bit and so on. It reduces the circuit complexity. Each full adder inputs a Cin, which is the carry of the previous full adder. Each carry bit "ripples" to the next full adder.

2) Basic unit: Initially Ripple carry adder structure is calculate for Cin = 0 the output of 13T full adder is given to the Proposed circuit and one of the input of that Proposed circuit is previous stage carry then it will provide the proper output by using 2T Multiplexer and 3T XOR gates structure. It is clear from the structure that it requires lesser area and consumes lesser power.

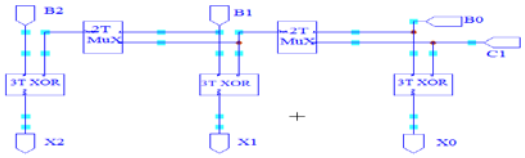


**Fig. 5.** Block Diagram of 3-bit proposed circuit

Aim of the proposed architecture is to reduce the overall latency. This result in increased in speed by using carry Select adder which reduce latency. Therefore the proposed structure reduced the overalllatency count from 18 to 5.The speed of the circuit is depends upon the latency of the circuit. The arrangement of the proposed structure is show in Fig. 6.

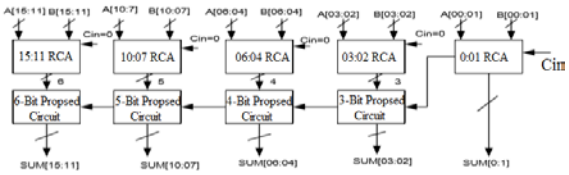


**Fig. 6.** 16-Bit Modified Carry Select Adder

16×16 Vedic Multiplier architecture is designed using four 8×8 Vedic multiplier modules, and three 16-bit modified Carry Select adder as shown in Fig.7. The 16 bit modified Carry Select adder are used for addition of two 16 bits and likewise totally three are use at intermediate stages of multiplier

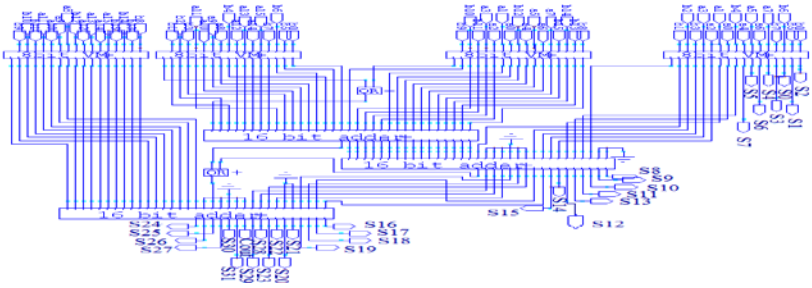

**Fig. 7.** Block Diagram of 16×16 Vedic Multiplier

The carry generated from the first adder is passed on to the next adder. The arrangement of the adders is such that delay decreases. The proposed Vedic Multiplier has low power consumption and high speed. It can be used for low power and high speed RISC Processor and digital signal processor.

## 5 Simulation Results

2×2, 4×4, 8×8,16×16 multiplieris designed and simulation is performed using H-spice. The simulation result for 16x16 bit Vedic multiplier is shown in table 3.

Table 1 shows the comparison between 8-bit proposed Vedic and Dadda Tree Multiplier. The latency defines the number of total phases required to compute the output.

**Table 1.** Comparison of Latency in Dadda Tree Multiplier and Proposed Vedic Multiplier

| STRUCTURE | Latency(ns) |
|---|---|
| Dadda Tree Multiplier | 18 |
| Proposed Vedic Multiplier | 5 |

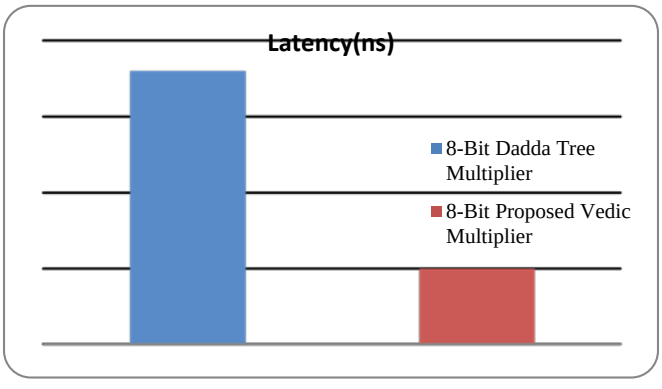


**Fig. 8.** Comparison of Latency of different Multiplier

Table 2 shows the power dissipation of various frequencies (100MHz and 400 MHz) at the constant power supply of 1.0v investigated.

**Table 2.** Comparison of the Power Dissipation of Various Multiplers

| STRUCTURE | 100 MHZ | 400 MHZ |
|---|---|---|
| Dadda Tree Multiplier | 5.09 mw | 15.12 mw |
| Proposed Vedic Multiplier | 1.35 mw | 1.79 mw |

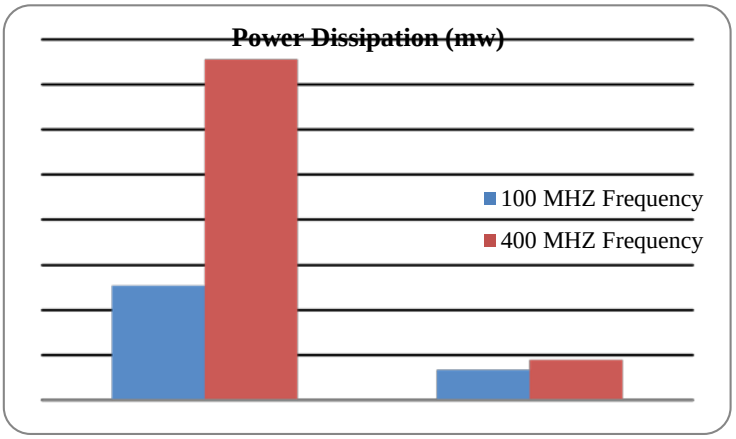


**Fig. 9.** Comparison of Power Dissipation of different Multiplier

Table 3 shows the simulation results of 8×8, 16×16bit Vedic multiplier at 1GHz frequency at the constant power supply of 1.0v investigated.

**Table 3.** Simulation Result for 8×8and 16×16 bit Vedic Multiplier

| Name | AveragePower (mw) | Latency (ns) | Delay (ns) | Leakage power (mw) | PDP (pj) |
|---|---|---|---|---|---|
| 8×8VM | 1.97 | 5 | 0.54 | 0.93 | 1.06 |
| 16×16VM | 6.08 | 6 | 0.73 | 2.49 | 4.43 |

## 6. Conclusion

The 16×16 Vedic multiplier is designed using Tanner EDA Tool 13.0. We have designed the 2×2 bit, 8×8 bit, 16×16 bit Vedic multipliers at 32nm technology. All the simulation results are carried out using H-Spice simulator.

The speed of the multiplier is decided by the latency of the circuit. The latency count is reduced from 18 to 5 that is 72.22% which is lesser with respect to the Dadda multiplier. The power dissipation at various frequencies (100MHz and 400MHz) at constant power supply 1.0v is investigated. The power dissipation reduced in proposed architecture due to use of modified carry select adder as compared to the Dadda multiplier. Result shows that the proposed architecture is more efficient in terms of the speed and power compared to the existing one. Result shows that proposed 16x16 bit Vedic multiplier has leakage power consumption 2.49mw, PDP is 4.43pj, delay is 0.73ns and average power dissipation is 6.08mw.The simulation results of proposed 16x16 bit Vedic multiplier are carried out with 1.0v at 1GHz frequency.

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