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High Performance Dynamic Full Adder Cell: A Comparative Analysis

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Abstract—In this paper we have presented three 1-bit full adder cells namely Conventional adder, Transmission gate based adder and 14T adder in dynamic logic style. One bit adder circuits are used to design 4-bit, 8-bit and 16-bit ripple carry adder circuit. In these circuits we have used clock to switch ON and OFF the circuit during evaluation and standby mode, respectively. It helps in improving the performance parameters as compared to the dynamic multi-output logic style in which two PMOS transistors are used to charge the outputs in precharge phase and one NMOS transistor to discharge the output during evaluation phase. Simulation result showsimprovements in delay, average power and PDP at 500MHz frequency at 32nm technology using 1.0 voltage supply. Result shows that among proposed dynamic adders 14T dynamic adder has best performance parameter as compared to conventional and transmission gate based adder.

Keywords: H.A(Half adder), CONV (Conventional), TG(Transmission gate), CMOS(Complementary metal oxide semiconductor), PDP(Power delay product).

1. INTRODUCTION

Full-adder is one of the core component of microprocessor and other complex circuits and is also used in various arithmetic operations for addition, subtraction, multiplication and accumulation. It is therefore inherent that the performance of the full-adder would affect the whole system [1], [2]. Therefore, much effort has been done to implement high-speed and low-power 1-bit full adder cells [3]. A full adder has three-input such as A, B and Cin where Cin is the carry input from previous block and two-outputs such as Sum and Cout [4]. Boolean equation describing the functionality of 1-bit full adder is:

$$Sum = A \oplus B \oplus Cin \quad \text{.....(1)}$$

$$Cout = A.B + A.Cin + B.Cin \quad \text{..... (2)}$$

A number of approaches have been adopted to implement a full adder circuit with low transistor count, low power consumption, high speed [5], [6]. The standard CMOS logic has high transistor count which consumes significantly larger area and power as compared to other pseudo-NMOS and passes transistor logic [7]. On the other hand dynamic logic style is an alternative logic style that uses a sequence of precharge and conditional evaluation phases governed by the clock to realize complex logic functions which leads to reduced delay thereby increased speed. In this approach N numbers of transistors are used to implement pull-up (PMOS) and pull-down (NMOS) network and 2 additional transistors for the clock signal which is used to switch ON and OFF the circuit during evaluation and standby mode respectively [8]. Advantages of dynamic logic are faster switching speed, lesser delay and full swing voltage levels [9]. Higher speed is the major advantage of dynamic logic due to its reduced delay as compared to static circuits. The main drawback is high power dissipation as compared to static logic due to higher switching activity. The average power consumption in a generic digital CMOS can be divided into three different components: dynamic, static (or leakage) and short circuit power consumption [10]. Switching power which includes both dynamic power and short circuit is consumed in charging and discharging of circuit capacitances during transistor switching. Leakage power is due to sub-threshold currents and reverse biased diodes in a CMOS transistor. Thus total power consumed in a CMOS transistor circuit is given by:

$$P_{avg} = P_{dynamic} + P_{short\text{-}circuit} + P_{static} \quad \text{.....(3)}$$

$$=V^2_{dd}.f_{clk}.C_L.\alpha + \alpha/12\ (V_{dd}- 2V_{th})^3 t_r/t_f + I_{stat}\ .V_{dd}$$

Where f_{clk} is the system clock frequency, C_L is the load capacitance, α is the activity factor, t_r/t_f is the rise and fall time of input signal, $I_{stat}$is the total current flowing through the device [11], [12].

In this paper we have presented three 1-bit full adder cells namely Conventional adder, Transmission gate based adder and 14T adder in dynamic logic style. In proposed dynamic adders we have used clock to switch ON and OFF the circuit. When circuit is in working state both PMOS transistor and NMOS transistor are ON by applying '0' to Clock 1 which is connected to PMOS transistor and by applying '1' to Clock 2 which is connected to NMOS transistor. On the other hand when the circuit is in stationary state both PMOS and NMOS transistors are OFF, this disconnect the path from VDD to Gnd. These full adders are optimized and simulated at 500MHz frequency. Dynamic and static adders are compared in terms of various parameters. The conventional dynamic full adder has 28 transistors to implement pull up and pull down network and 2 additional transistors for the clock signal. The transmission gate based adder has 20 transistors to implement pull up and pull down network and 2 additional transistors for the clock signal. The 14T full adder in case of dynamic style requires 2 more transistors for the clock signal; in total it has 16 transistors [13]. The rest of the paper is organized as follows: Section II, present our proposed designs. In Section III, simulation results are shown. Finally Section IV contains a conclusion.

I. THE PROPOSED FULL ADDER CELLS

In static logic families the pull up and pull down networks operate concurrently whereas a dynamic logic uses a sequence of precharge and conditional evaluation phases governed by the clock to realize complex logic functions. The operation of dynamic logic can be divided into two major phases: working and stationary state. When Clock1=0 and Clock2=1 circuit is in working state and when Clock1=1 and Clock2=0 circuit is in stationary state[14].

A. Design I

Conventional dynamic CMOS full adder as shown in Fig.1 has 28 transistors and additional 2 transistors for the clock signal, is the complementary CMOS structure which combines transistor PMOS pull-up and transistor NMOS pull-down network to produce the output [15].

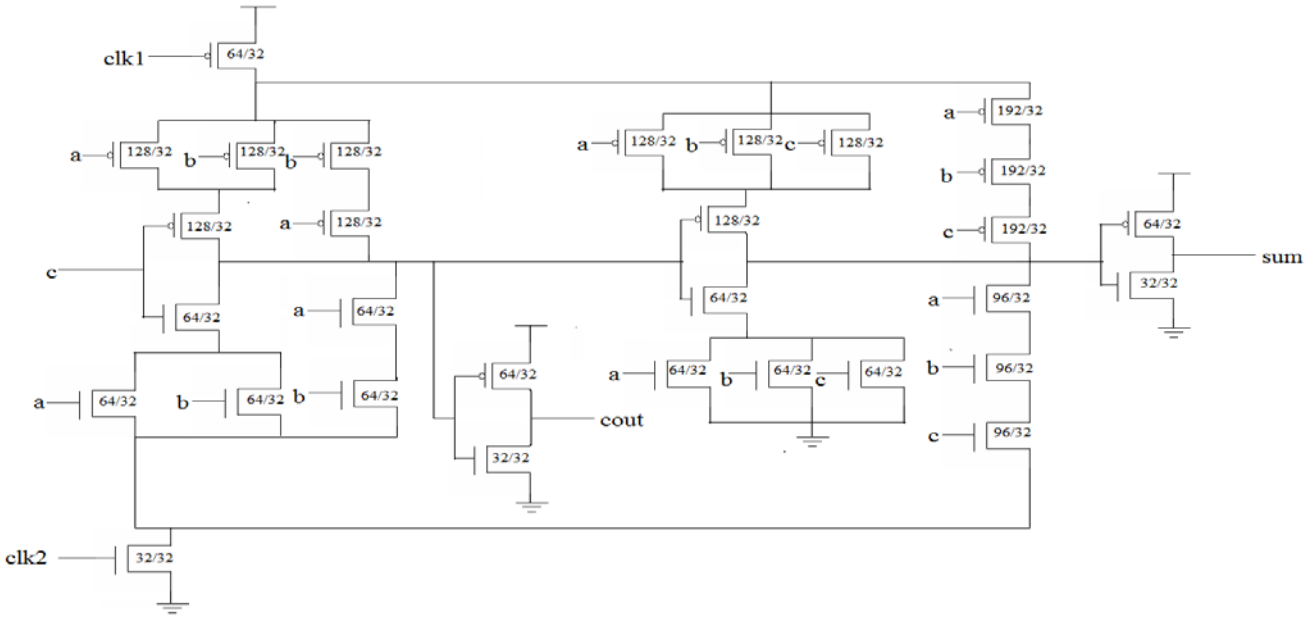

Fig. 1Conventional Dynamic Full Adder Cell

B. Design II

The transmission gate dynamic full adder cell as shown in Fig.2 is based on transmission gate and has 20 transistors plus 2 additional transistors for clock signal.

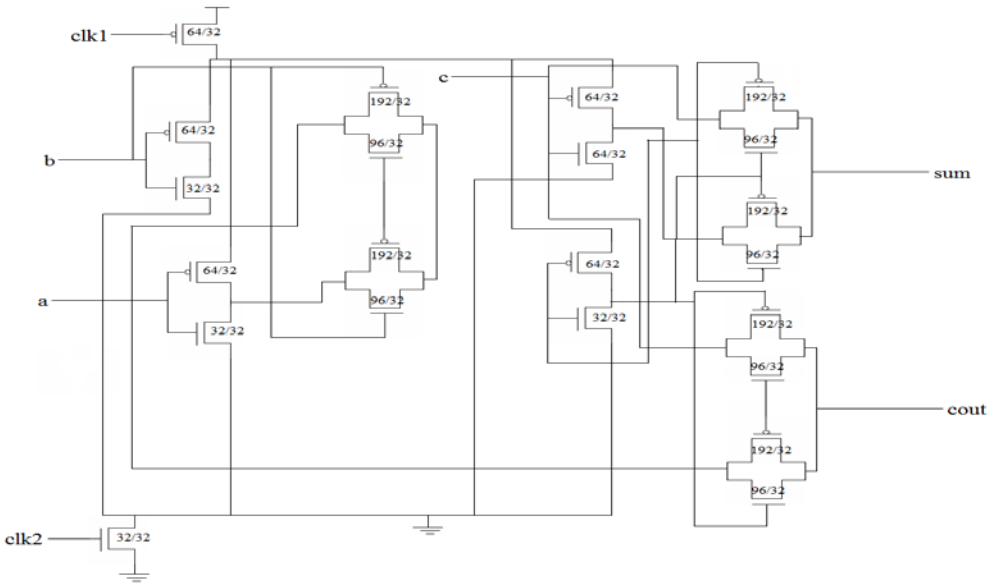

Fig. 2Transmission Gate Dynamic Full Adder Cell

C. Design III

The third design is introduced with the aim of enhancing the first two designs. 14T dynamic adder as shown in Fig.3 has 14 transistors to implement pull-up and pull-down networks plus 2 additional transistors for clock signal [16].

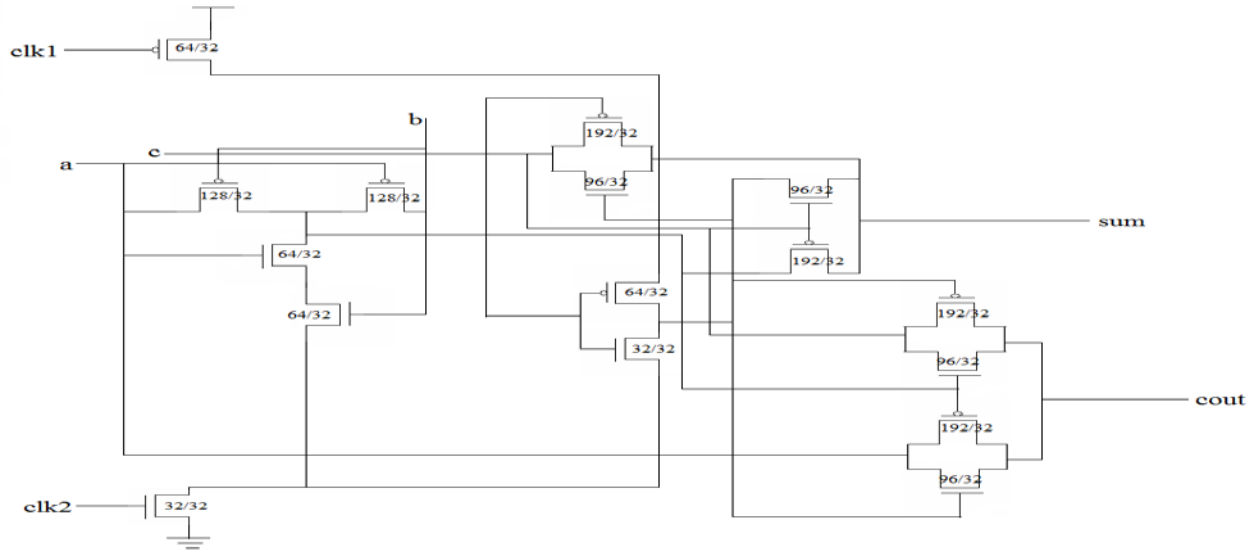

Fig. 314T Dynamic Full Adder Cell

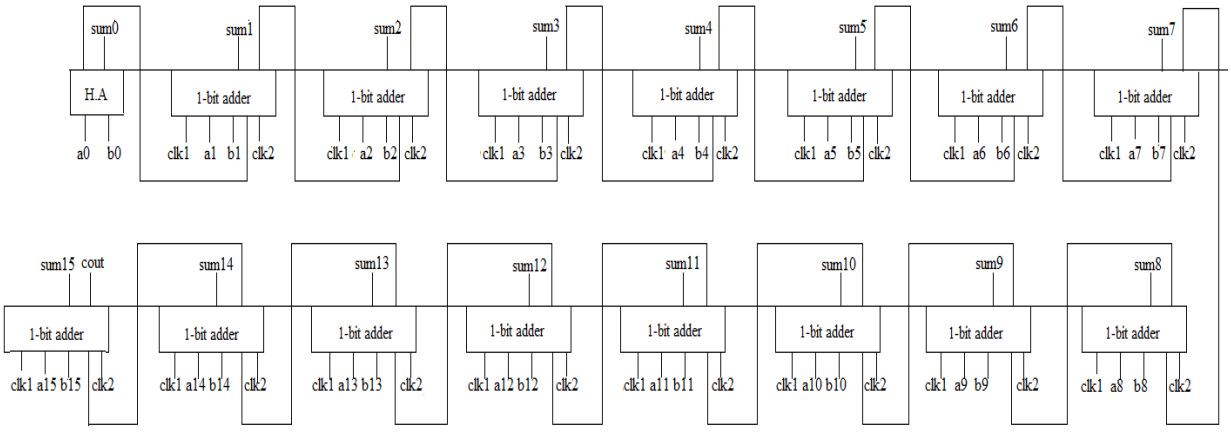

Fig. 4 16-bit 14T Dynamic Full Adder

2. THE SIMULATION RESULTS

The proposed designs and other three full adder cells (Conventional CMOS, Transmission gate CMOS and 14T full adder) all are simulated using Tanner EDA tool V13.0 at 32nm CMOS technology [17] at roomtemperature using 1.0v voltage supply at 500MHz frequency. In case of dynamic logic, results are obtained during working phase when Clock1=0 and Clock2=1.The output signal waveform for 1-bit and 16-bit 14T dynamic adder at power supply of 1.0v is shown in Fig.5 and Fig.6 respectively. The frequency of clock signal is 500MHz. The leakage power in each full adder cell is calculated by assuming firstly all inputs '0' then '1'.The delay parameter is calculated from the time that clock signal reaches 50% of the input to the time that output reaches the same voltage level. The average power consumption is termed as total power consumed during all transitions. Finally the power delay product (PDP) is the multiplication of maximum delay and average power consumption (PDP =Maximum Delay * Average power of circuit). The results for delay, average power consumption and PDP are separately illustrated in Fig.7, Fig.8 and Fig.9.

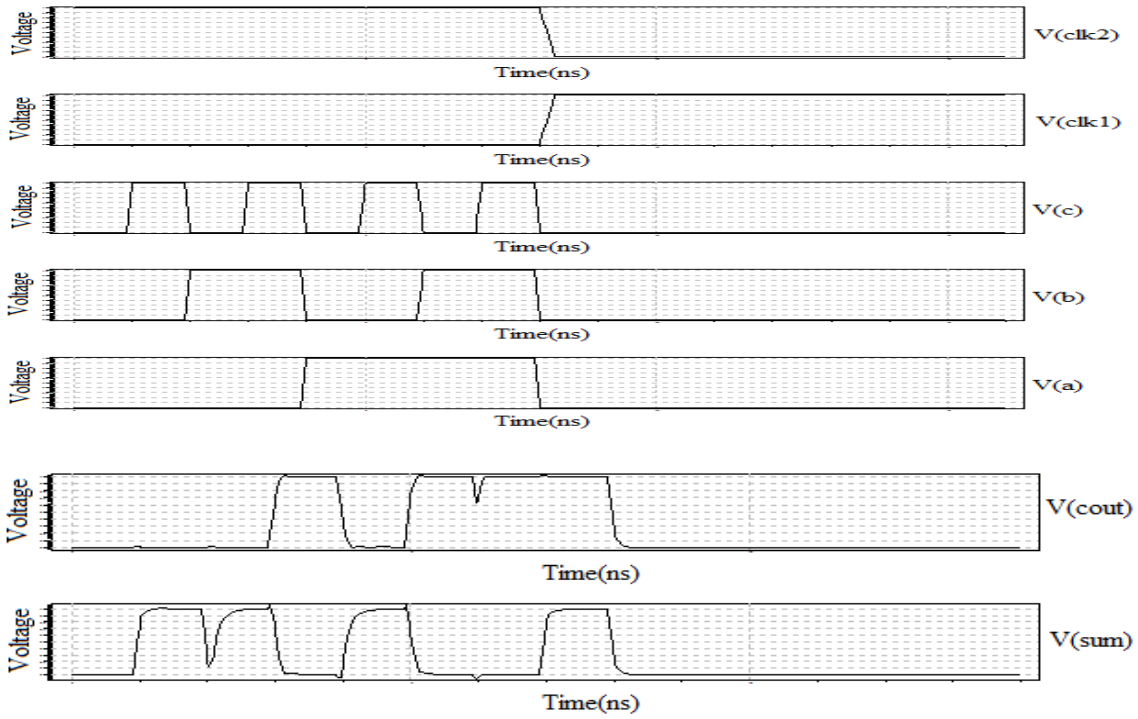

Fig. 5 Input and Output Signals for Proposed 1-bit 14T dynamic full adder cell at 1.0v and 500MHz frequency.

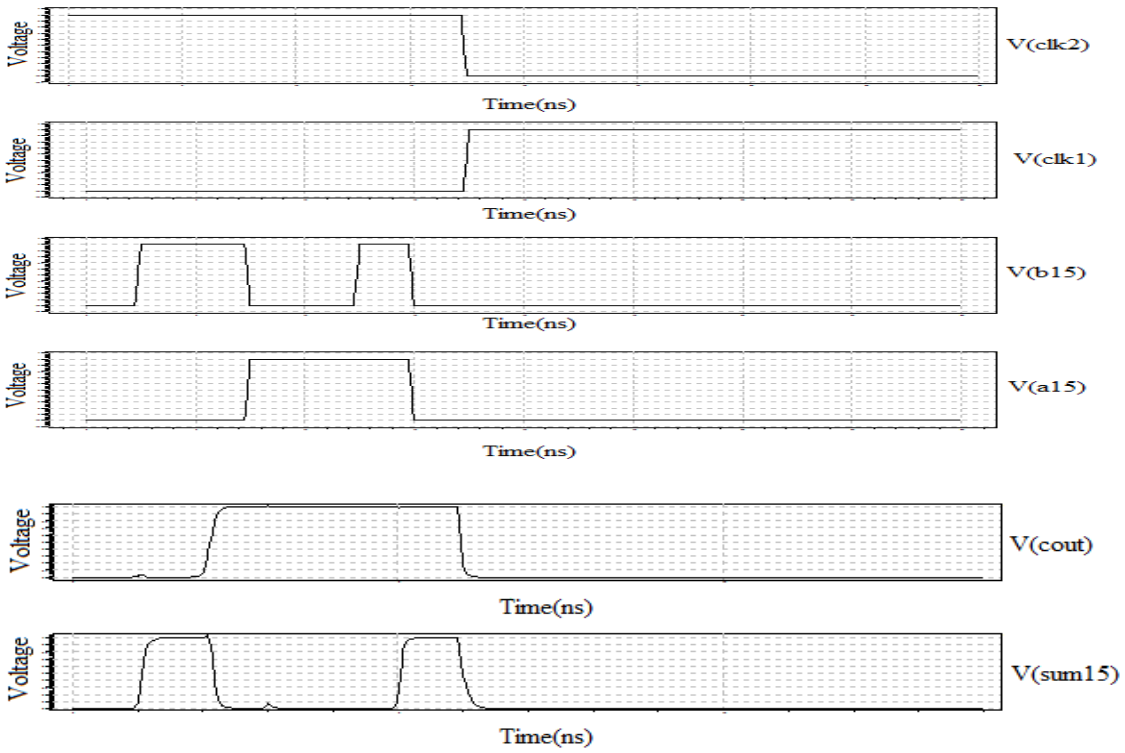

Fig. 6 Input and Output Signals for Proposed 16-bit 14T adder design at 1.0v and 500MHz frequency.

The results of 1-bit proposed adders are shown in Table I at 1.0v supply voltage and 500MHz frequency. Result shows that Conventional Dynamic Full adder Cell has 38.1% lower PDP as compared to Conventional CMOS adder, 14T Dynamic Full Adder Cell has 50% lower PDP as compared to 14T adder. Among these 1-bit dynamic adders 14T dynamic adder has better performance parameters. It has 66.6% less leakage power as compared to conventional dynamic adder and 48% less leakage power as compared to transmission gate dynamic adder. It consumes 92.8% less power as compared to conventional dynamic adder and 89.5% less power as compared to transmission gate dynamic adder. It has 94.1% lower PDP value as compared to conventional dynamic adder and 90.6% less PDP as compared to transmission gate dynamic adder. In case of 16-bit dynamic adders 14T adder consumes 78.4% less power as compared to conventional dynamic adder and 68.0% less power as compared to transmission gate dynamic adder. It has 79.3% less PDP as compared to conventional dynamic adder has 71.0% less PDP value as compared to transmission gate dynamic adder.

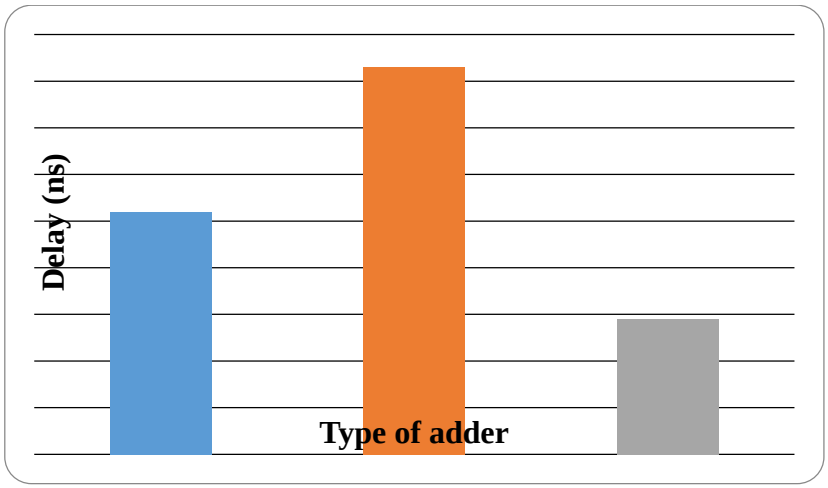

Fig. 7 Delay of 16-bit dynamic full adder cells at 500MHz frequency

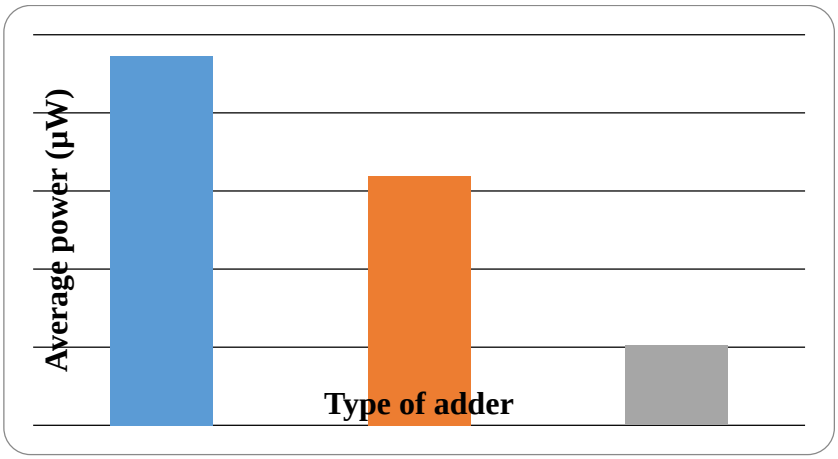

Fig. 8 Power Consumption of 16-bit dynamic full adder cells at 500MHz frequency

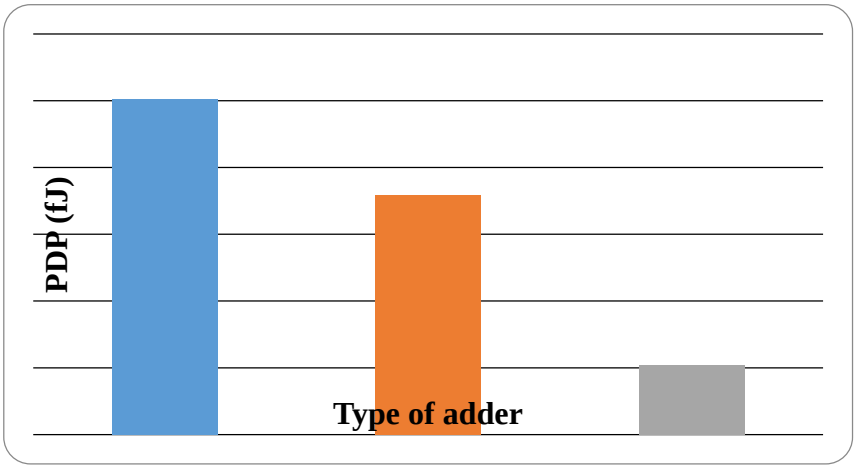

Fig. 9 Power delay product of 16-bit dynamic full adder cells at 500MHz frequency

TABLE I:
Comparison of 1-bit adders at 1.0v and 500MHz frequency

Type of adder	Leakage power(µW)	Delay (ns)	Average power(µW)	PDP (fJ)
Conv	0.19	0.243	4.56	1.10
TG	0.28	0.125	2.97	0.37
14T	0.09	0.253	0.34	0.08
Conv Dynamic	0.39	0.196	3.50	0.68
TG Dynamic	0.25	0.167	2.59	0.43
14T Dynamic	0.13	0.178	0.27	0.04

TABLE II:
Comparison of 16-bit dynamic adders at 1.0v and 500MHz frequency

Type of adder	Leakage power(µW)	Delay (ns)	Average power(µW)	PDP (fJ)
Conv Dynamic	3.99	0.532	47.3	25.1
TG Dynamic	3.99	0.563	31.9	17.9
14T Dynamic	2.11	0.509	10.2	5.19

3. CONCLUSION

Three different 1-bit static and dynamic adder styles named as conventional, transmission gate and 14T full adder are designed and analysed for various performance parameters. Result shows that PDP of dynamic adders is less as compared to static adders. However transmission gate adder style has somewhat larger PDP. This is due to higher delay but average power is in acceptable limit. Among these three dynamic adder styles 1-bit 14T adder has 94.1% and 90.6% less PDP than conventional dynamic and transmission gate dynamic adder respectively. It gives better performance in terms of leakage, average power consumption and delay. In case of 16-bit dynamic adders 14T adder has 79.3% and 71.0% less PDP as compared to conventional and transmission gate adder respectively.

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