Survey on Power Minimization Techniques in Digital Systems

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Abstract- Power has become one of the circuit implementation bottleneck for modern integrated design. As technology advances, system on chip can have more and more components that lead to higher power density. This paper includes the survey onvarious techniques used for implementation of low power systems.

Keywords: Integrated design, system on chip, power density, low power systems.

1. Introduction

Today's microprocessors consume from few 100mW to 100W power. More than half of the power is dynamic in nature. The clocks contribute the major of the dynamic power. Dynamic power refers to the power dissipation related to the active components in the circuit. The dynamic power in clock is attributed to interconnect capacitance of clock nets, gate capacitance of sequentials and gate and diffusion capacitance of clock buffers.Various clustering techniques were employed for power minimization so far including use of multi-bit flip-flops and pulsed latch. The multi-bit flip-flop creation from single-bit flip-flop design and replacement of those to save power was proposed.

Then multi-valued logic circuits were introduced using fuzzy logic for reducing the hardware which will have positive effects in power minimization. Earlier, multi-valued logic design using carbon-nanotube field-effect transistors were introduced to improve the performance and lower the power dissipation.

Section 2 deals with the literature survey which covers the research of span 2005-2015. Future Scope is discussed in section 3 of the paper.

2. Literature Survey

A. Raychowdhury *et al.* introduced multi-valuedlogic design using carbon nano-tube field-effect transistors and comparison in terms of power and performance was done. The power-delay product was seen to be 22% more in complementary adder than in ternary adder in 2005 [1].

R.S.Shelar examined the clocks as major source of power consumption in digital circuits. He proposed a clustering algorithm for minimization of power in local clock tree and aimed at minimizing the interconnect capacitance in local distribution of clock inside the block which was responsible for power loss. It employed the clustering algorithm for duplication of clock buffers. The algorithm resulted in power saving of 14% and 2.5x speed up. Thus power cost was reduced by 32% in 2012 [2].

S.Huan Wang *et al.* proposed merging of flip-flops to multi-bit flip-flop to reduce clock network size, switching power of the net (reduction of clock buffers), switching power of interconnect (reducing the wire-length)and hence the total power consumption. Further the multi-bit flip-flops were relocated while taking into consideration the time and placement density constraints. Approach of multi-bit flip-flops was based on computation of maximal cliques in rectangular intersection graph. K-bit multi-bit flip-flops were made from

clique and were frequently updated. Here experimentally, number of clock sinks were reduced by 59%-74% and total switching by 24%-29% in 2012 [3].

M.P.Lin *et al.* focused multi-bit flip-flops are effective to save power consumption for System on chips (SoCs). It introduced the Progressive Window-Based Optimization Technique to reduce placement deviation and improve runtime efficiency. Methodology involved was flip-flop grouping in which groups were made according to time slack constraint and flip-flop placement which introduced coordinate system, placement and interconnecting wire-length and Progressive Window-based Optimization in 2011 [4].

I.H.Jiang *et al.* focused on the post-placement multi-bit flip-flop clustering. Utilizing the properties of Manhattan Distance and coordinate transformation, the problem by interval graphs and uses pair of linear-sized sequences was modeled. Identification of partial sequences in combination marked it fast in 2012. Total clock power reduction was reported to be 30.09%. Clock subtrees, clock buffers, clock depth were also reduced in the paper [5].

Y.Shyu *et al.* introduced the power reduction by merging the flip flops to Multi-bit flip flop by transforming the coordinate system. It utilized the concept of pseudo type to enumerate all possible combinations in combination table thereby reducing the time complexity. It introduced the concept of Manhattan Distance. Besides power reduction, it had focused on wire length reduction and cost factor. Algorithm reduced the power by 20-30%. Timing was so reduced that for 1.7 million flip-flops it took five minutes to replace the flip-flops in 2013 [6].

U.K.Malvia and V.Tripathi proposed the design of new fuzzy memory cell of four logic levels which can hold Logic0, Logic1, Logic2 and Logic3. The multi-level logic design had reduced the hardware and hence the clock sinks in the design. For storing any decimal value range 0 to 255 in binary logic eight flip-flops were required but when four level logic was used, only four flip-flops stored the desired values in 2013 [7].

B. Choi focused on the advancing from two to four valued logic thereby decreasing the hardware and increasing the speed of computation. It had introduced the designing of the four-valued NOT,AND,OR gates and D-flip-flop and hence increased the efficiency of the circuits in 2013 [8].

B.Choi and K.Shukla aimed at designing and implementation of digital circuits entirely within the domain of multi-valued logic. In a four-valued logic circuit, each wire carried two bits at a time, each logic gate operated two bits at once, and each memory cell recorded two bits at one time. To make the multi-valued computation possible, they described a simple four-step process for designing multi-valued circuits to implement any multi-valued functions. The design of a four-valued adder was provided as an example. They also contributed new designs for multi-valued memory and flip-flops, which can be extended to be used for infinite-valued or Fuzzy logic circuits, for fully exploiting many-valued logic and fuzzy paradigm in hardware. The multi-valued circuit design methodology and the multi-valued memory provided the necessary and sufficient tools and components for designing multi-valued systems entirely within the domain of multi-valued logic in 2015 [9].

3. Conclusion and Future Scope

Power-Optimization got importance in digital circuits not only because of cost but also due to the reliability issues. This survey has been focused on power-optimization aiming at minimizing clock tree power by minimizing the interconnect capacitance. This work was enhanced by lowering the clock buffers and controlling the switching power[2]. Then, this target was achieved by merging of single bit flip-flops to multi-bit flip-flop[3].Introduction of the post-placement power-optimization where progressive window-based optimization technique was done to minimize consumption and interconnecting wire-length while taking into consideration timing and placement constraints[4].
The work is taken to multi-valued logic on reducing the hardware, improving the computation speed of flip-flops[7]. The work is extended by advancing from two to four-valued logic circuits, allowing the future

development in memory cells and flip-flops[8]. Moving to multi-valued logic circuit design and implementation[9], the work is to be done to introduce infinite-valued flip-flops thereby reducing the hardware and it will be further utilized in power-optimization atintegrated circuit level in future. Future scope lies in reduction of flip-flops due to multi-logic and thereby leading to operations minimization which is supposed to reduce power consumption considerably. Earlier power reduction methods using multi-valued circuits involved nano-technology, now multi-valued circuits will be devised using fuzzy logic whose quantitative analysis is yet to be done.

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