Anubhav Sharma[1], Shashank Kamthan[2], Aby K George[3], Amjad Almatrood[4,] Harpreet Singh[5], Harinder Pal Singh[6]

On development of Chip to Control Laser Time for Cell-selective Arrhythmia Ablation of Heart

Anubhav Sharma[1], Shashank Kamthan[2], Aby K George[3], Amjad Almatrood[4,] Harpreet Singh[5], Harinder Pal Singh[6]

[1, 2,3,4,5]College of Engineering, Wayne State University, Detroit, MI, USA

[6]Dept of Technical Education, Government of Punjab, India

Email: [1]asharma.ie@wayne.edu, [5]hsingh@eng.wayne.edu

Abstract. Human heart is a very important part of body. Its proper functioning is extremely important for the survival of human being. Quite often, the heart does not function properly owing to one reason or the other. The primary reason for such a malfunctioning of heart could be due to some of the faulty and abnormal cells in heart. Generally, the photo-techniques are used to destroy such abnormal cells. However, such techniques are not much effective. Currently, laser techniques are used to destroy malfunctioning cells of the heart. The basic idea about these techniques is that with the help of a laser beam, some particles are sent to the cells of heart, so that only the abnormal cells get destroyed while retaining the normal or healthy cells of the heart. Further, the paper also demonstrates a procedure for applying a laser beam for a specified time. The procedure is developed in Verilog software. The Verilog program is then implemented on Field Programmable Gate Array (FPGA), and the testing of this program is done. The developed circuit in the present paper is expected to be useful for a number of applications indifferent industries.

Keywords. Digital Chip,MATLAB, HDL, Cadence, FPGA,Laser beam, Ablation of Heart .

1. Introduction

Recently in a paper authored by Avula et al.[1], use of laser in a surgical procedure is reported on rodents. Such types of laser techniques[4] are being extensively used for destroying the abnormal cells and retaining normal cells. Since the invention of laser in 1958, it has significantly contributed in the development of different areas such as manufacturing[5], medical, communication [6] [7]etc. There are large numbers of commercially available lasers in the market. The subject of laser has attracted the attention of engineers and scientists around the word to apply them successfully in different applications.

It has been observed that a large number of lasers are available in commercial market. However, it depends on the application for which the laser is to be used. The main focus of this work of is to develop a laser chip which can be used in laser assisted surgery procedures. This paper deals with laser applications[2] [3]in surgery. In particular, it is related to laser timefor Cell-selective arrhythmia ablation of heart[4]. The objective is to develop a laser chip, which controls the laser light to strike unwanted cells of heart while at the same time, not damaging the normal cells.

Thus, the main objective here is to use laser to act for 3 cycle times[6]. The cycle time of course can be varied depending on the specific case. The laser beam is on while the button is ON and then laser get stopped after 3-time cycle. The important feature here is that even if the doctor presses the button, by mistake, the laser will continue[7]. This type of chip is proposed to be developed here.

METHODOLOGY AND ALGORITHM OF CHIP DEVELOPMENT

The steps for the development of Chip are given as below:

- Write down the state table for the Arrhythmia Application
- MATLAB Implementation

- Implement the state table using State flow – State chart machine in Simulink
- Compile using RTW (Real Time Workshop – Embedded Coder)
- Simulate State machine model using MATLAB Simulink Test Vector
- Use HDL Coder Tool to generate the code in Verilog for the example under consideration

• Xilinx – FPGA Implementation

- Import the Verilog code generated by MATLAB tool
- Synthesize the code to check the error
- Implement the Verilog code including IO mapping with XC3S700 – Spartan 3A/AN FPGA structure
- Generate Programming Code
- Simulate (Pre simulation process) by ISIM (Xilinx Integrated Simulator)
- Compare the results with reference to MATLAB simulation result
- Load FPGA program to Xilinx FPGA chip
- Post simulation on FPGA board and validate state chart results

• Cadence Implementation

- Import the Verilog code generated by MATLAB HDL Coder and Test case used in FPGA Pre simulation
- Compile both Main code and test case in NCLAUNCH
- Elaborate the Verilog code
- Open Cadence Simulation of Test case by NCSIM (NC Simulator)
- Validate the results with reference to Xilinx Simulation results and MATLAB simulation results
- Modify encounter IO file to incorporate PADS for Input, Output and VDD/ VSS
- Import Verilog code in Encounter
- Modify width and Length of wire and Metal frame based on 45 nm Chip design
- Add Floor plan and Nano Route it
- Verify Geometry to check any mismatch in Encounter Design
- Generate DEF file from Encounter
- Open virtuoso and import DEF file generated from Encounter
- Plugin to PVS and Run PVS DRC check

I. IMPLEMENTATION OF ALGORITHM FOR CHIP DEVELOPMENT

The above algorithm is implemented as follows:

• The state machine diagram is defined below in Fig 1. It consists of 4 states and single input – single output. The input ("b") is given by the surgeon, the output ("x") defines laser beam. Fig 2 shows the state table implementation in Stateflow-Statechart window in MATLAB Simulink. Fig 3 shows the outer layout of MATLAB model

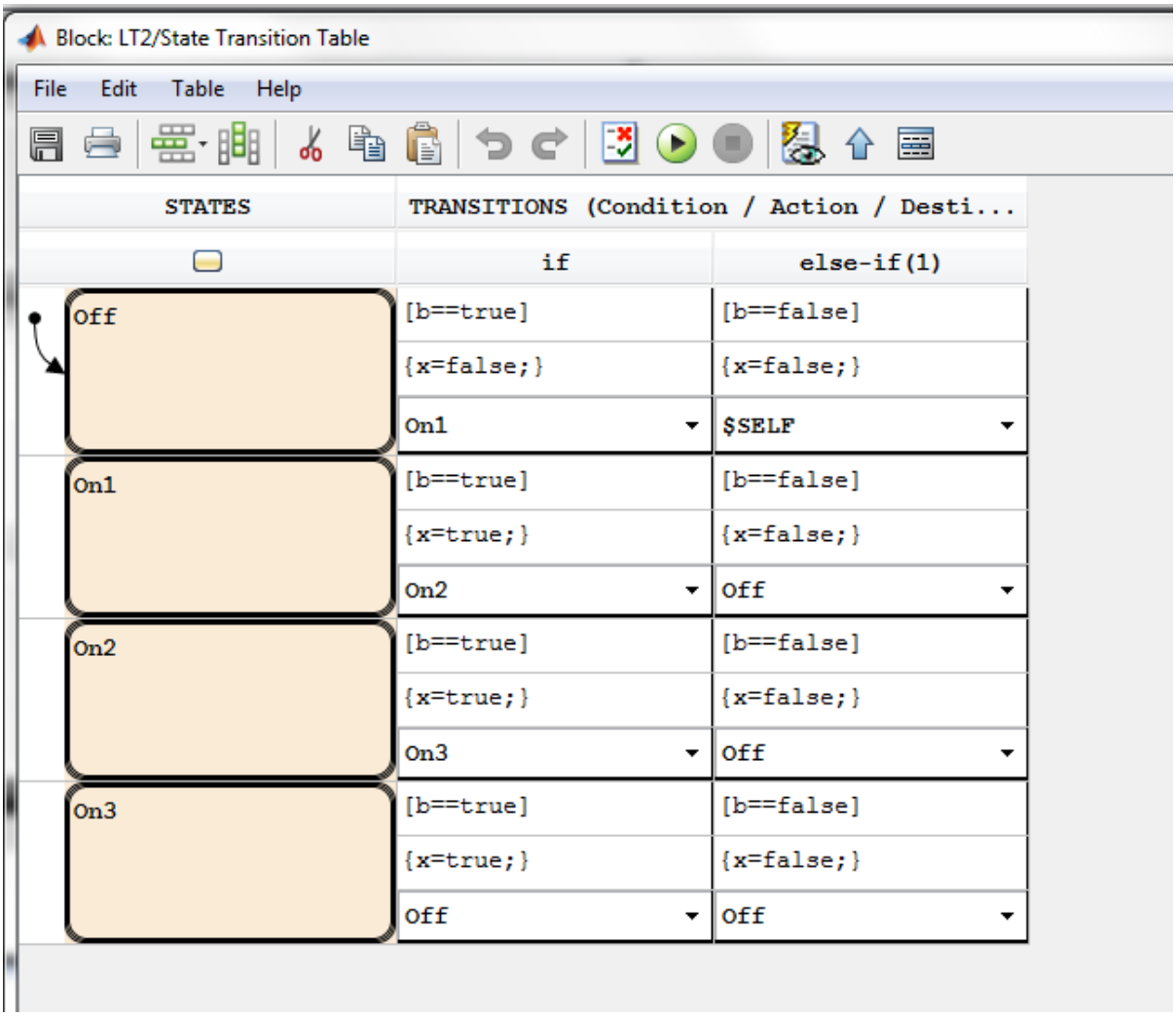

Fig 1. State machine using state flow in MATLAB simulink

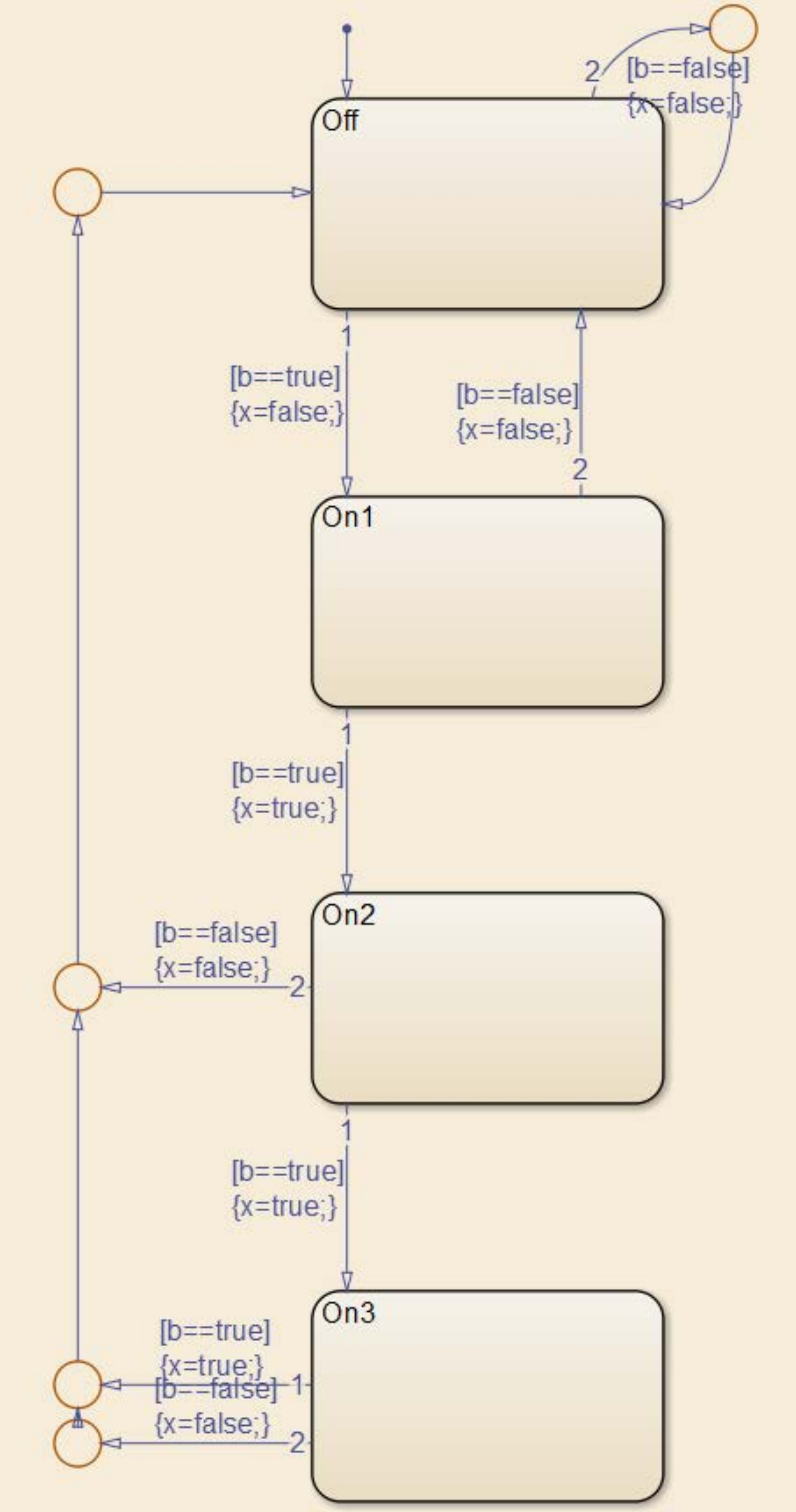

Fig2.State table

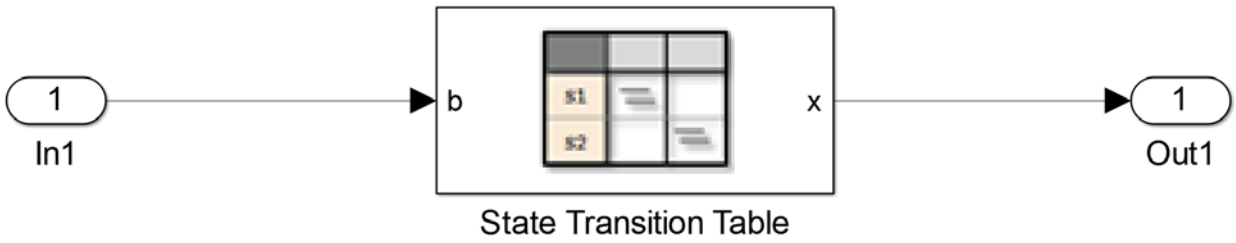

Fig 3. Layout of Simulink – state flow model (i.e., "In1" represents "b" and "Out1" represents "x")

- The code generated by HDL Coder (MATLAB – RTW) is given in Appendix.
- The results of FPGA Implementation are given in Fig 4. FPGA Board Description is Spartan 3- XC3S700. All the states were tested by giving inputs and verifying binary inputs and binary outputs as per state table

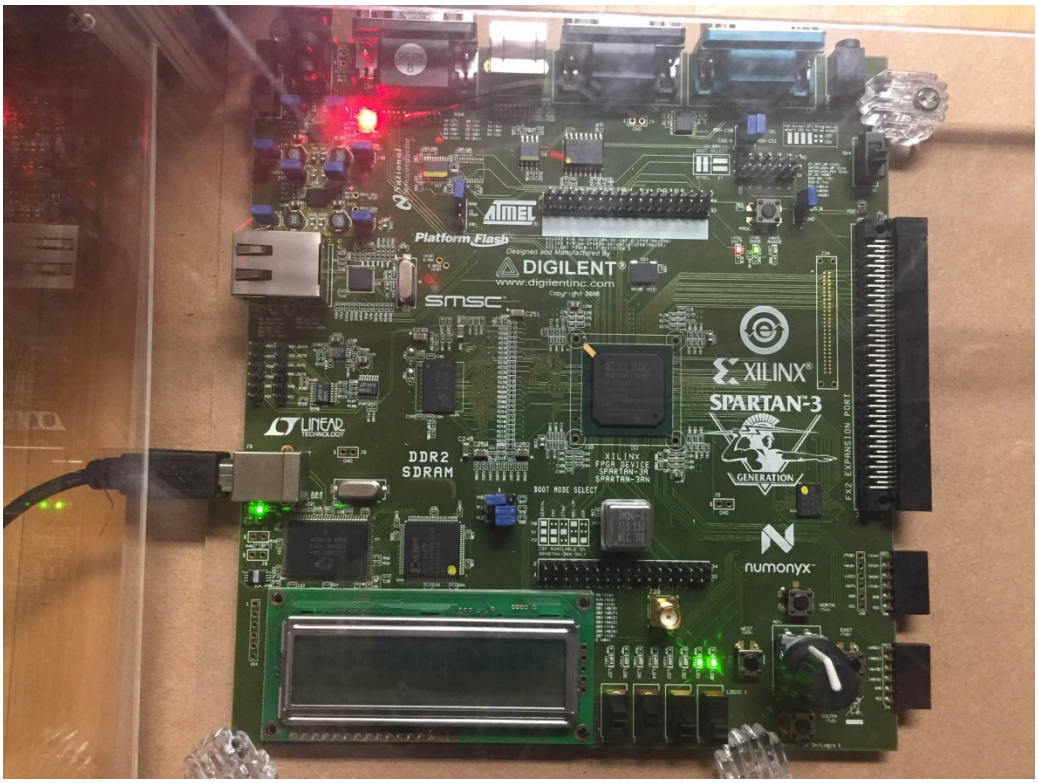

Fig 4. FPGA simulation on Spartan 3A/AN – XC3S700A

- The simulation is also verified with the help of ISIM (Xilinx Simulator) and NCLAUNCH (NCSim) by Cadence[8] installed on Linux Machine. Fig 5(a)and Fig. 5(b) shows the result of simulation via ISIM and NCSim respectively.

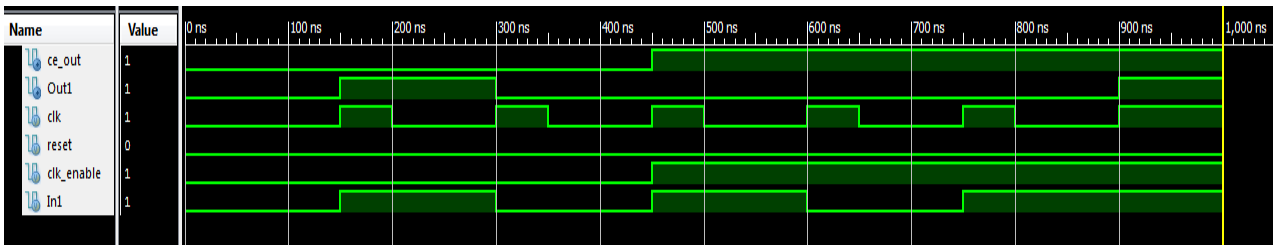

Fig 5(a). Simulation result using ISIM (Xilinx)

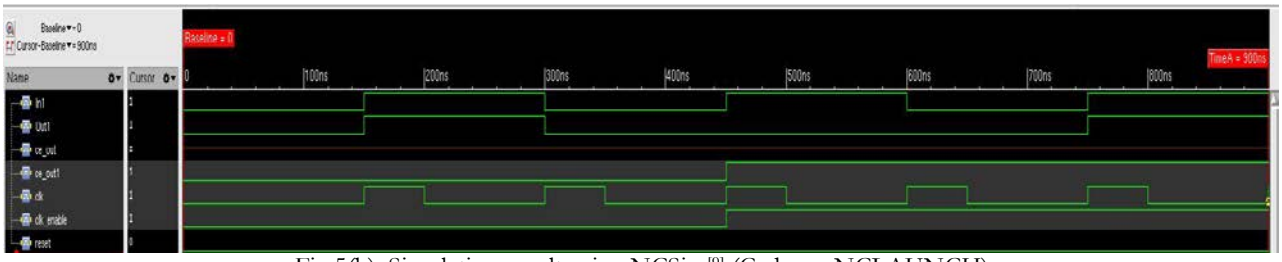

Fig 5(b). Simulation result using NCSim[9] (Cadence NCLAUNCH)

- The design rules [10] [11] were verified using Encounter and Virtuoso (64 bit). Fig 6 shows the implementation of Digital chip under 45nm design rules. This figure also includes the PADS for all the input, Output, VDD and VSS.

Fig 6. Digital chip in virtuoso including padframe

We used 45 nm Technology[8] [9] .The design is tested and it can be sent to any silicon foundries for fabrication. Once we get the chip back from foundry, it can be tested for all the possible cases. Please note that the testing of VLSI chip is the very involved task and requires high priced testers.

2. RESULTS AND ANALYSIS

Simulations of the proposed chip are given in this paper. The simulation has been done for both Pre-Simulation (i.e., Simulink Test Vector, Xilinx ISIM and Cadence NCLAUNCH) and Post Simulation (i.e., FPGA Spartan 3 A/AN – XC3S700 board).A sequential model of the proposed Laser Beam is given in the form of sequential machine. The sequential machine is represented in the MATLAB. With the help of HDL coder, Model is translated in automated generated Verilog code. This code is then implemented in the form of the Chip design. This design can be sent to MOSIS for fabrication. In this work, we have tested the simulation of sequential circuit proposed and verified the working of the circuit with the help of FPGA. The simulation diagrams in this paper show both the pre-simulation and post-simulation (using FPGA). Technology used here is 45nm design implementation. The 45nm technology is more expensive than 500 nm technology and is generally not encouraged by universities because of high fabrication cost by MOSIS[10]. The MOSIS

is an NSF sponsored fabrication facility. Mainly, it accepts 500nm technology for educational purposes. Once the design of Laser beam is more close to reality, such chips can be developed, got fabricated and tested real-time.

3. Conclusions

The applications of laser are extremely important and are becoming more and more as evidenced by a large number of papers in this area. Recently a paper by Avula et al. [1] suggests its application in destroying the unwanted tissues of heart. In this paper we have developed a procedure by which one can develop a laser chip for this purpose. The procedure has been tested on FPGA. Please note that this paper only discusses an approach for designing and fabricating. The chip is designed here for cell selective arrhythmia ablation for heart. The chip designed here is far from real chip, which could possibly be used for such an application. Design of such a chip will be quite involved. However, the procedure suggested here will be helpful for any research worker who wants to develop real chips. It is hoped that such chips would be useful for the problem of arrhythmic heart in particular and a large number of health problems in general. We do hope to continue future work and collaboratewith research workers in this area.

References

[1] R, Avula, Uma Mahesh, et al. Science Translational Medicine: Cell-Selective Arrhythmia Ablation for Photomodulation of Heart Rhythm. 7 Vol. American Association for the Advancement of Science, 10/28/2015. Web. 12 Dec. 2015.

[2] Vahid, Frank. Digital Design with RTL Design, Verilog and VHDL. John Wiley & Sons,2010

[3] OumtaYoukhana, Developing a Digital Circuit to Control Laser Time, Poster IEEE Humanitarian conference , 2015

[4] Image LBW:http://www.basqueresearch.com/new/laser-welding-enables-recovery-deteriorated-parts-of-high-added-value-for-aeronautics-sector

[5] Image Laser cutting:https://www.luxexcel.com/3d-printing/laser-die-cutting/

[6] Image Communications: http://www.jpl.nasa.gov/spaceimages/details.php?id=PIA07499

[7] Developing a digital circuit to control Laser Time for Industrial Applications, IEEE SEM Fall 2015 – November 17, 2015

[8] Cadence Help User Guide, Product Version 2.0, Cadence Design Systems, Inc., San Jose, CA, 2012.

[9] Cadence Application Infrastructure User Guide, Product Version 6.1.5, Cadence Design Systems, Inc., San Jose, CA, 2012

[10] MOSIS Scalable CMOS (SCMOS) Design Rules, Revision 8.00, The MOSIS Service, Marina del Rey, CA, May. 2009.

[11] Virtuoso Layout Suite XL User Guide, Product Version 6.1.5, Cadence Design Systems, Inc., San Jose, CA, May. 2012.

APPENDIX

```
moduleState_Transition_Table (clk,reset,enb,b,x);
inputclk; reset; enb; b;
output x;
parameteris_State_Transition_Table_IN_Off = 2'd0, is_State_Transition_Table_IN_On1 = 2'd1,
is_State_Transition_Table_IN_On2 = 2'd2, is_State_Transition_Table_IN_On3 = 2'd3;

reg [1:0] is_State_Transition_Table; x_reg; [1:0] is_State_Transition_Table_next; x_reg_next; guard1_1;
always @(posedgeclk or posedge reset)
begin : State_Transition_Table_1_process
if (reset == 1'b1) begin
is_State_Transition_Table<= is_State_Transition_Table_IN_Off;
```

```
end
else begin
if (enb) begin
is_State_Transition_Table<= is_State_Transition_Table_next;
x_reg<= x_reg_next;
end
end
end
always @(is_State_Transition_Table, b, x_reg) begin
is_State_Transition_Table_next = is_State_Transition_Table;
x_reg_next = x_reg;
   guard1_1 = 1'b0;
case ( is_State_Transition_Table)
is_State_Transition_Table_IN_Off :
begin
if (b == 1'b1) begin
x_reg_next = 1'b0;
is_State_Transition_Table_next = is_State_Transition_Table_IN_On1;
end
else if (b == 1'b0) begin
x_reg_next = 1'b0;
is_State_Transition_Table_next = is_State_Transition_Table_IN_Off;
end
end
     is_State_Transition_Table_IN_On1 :
begin
if (b == 1'b1) begin
x_reg_next = 1'b1;
is_State_Transition_Table_next = is_State_Transition_Table_IN_On2;
end
else if (b == 1'b0) begin
x_reg_next = 1'b0;
is_State_Transition_Table_next = is_State_Transition_Table_IN_Off;
end
end
     is_State_Transition_Table_IN_On2 :
begin
if (b == 1'b1) begin
x_reg_next = 1'b1;
is_State_Transition_Table_next = is_State_Transition_Table_IN_On3;
end
else if (b == 1'b0) begin
x_reg_next = 1'b0;
is_State_Transition_Table_next = is_State_Transition_Table_IN_Off;
end
end
default :
begin
if (b == 1'b1) begin
x_reg_next = 1'b1;
          guard1_1 = 1'b1;
end
```

```
else if (b == 1'b0) begin
x_reg_next = 1'b0;
        guard1_1 = 1'b1;
end
end
endcase
if (guard1_1) begin
is_State_Transition_Table_next = is_State_Transition_Table_IN_Off;
end
end
assign x = x_reg_next;
endmodule  // State_Transition_Table
```