On the development of Arithmetic Processors

Sairam Gowrisankar[1], Amjad Almatrood[2], Aby K George[3], Harpreet Singh[4], Harinder Pal Singh[5]

[1,2,3,4]College of Engineering, Wayne State University, Detroit, MI, USA

[5]Dept of Technical Education, Government of Punjab, India

Email:[1]fn4309@wayne.edu, [4]hsingh@eng.wayne.edu

Abstract—Therehas always been anincreasing interest in the development of new arithmetic processors. The objective of this paper is to describe the hardware implementation of a pipelined arithmetic processorpublished previously, which can add, subtract,multiply,divide,square and square root the binary numbers. The processor described resulted in 46input/output pins.The MOSIS and cadence fabrication technology generally allow up to 40 pins. In this paper hardware implementation of arithmetic processor is taken up so that processor chip can be developed by 40 pins. This hardware implementation will lead to better implementation of handling input, output pins for future processors. The hardware implementation of the modified array has been done using Simulink and tested. It is hoped that this research will lead to the design and VLSI implementation of new arithmetic processor.

Keywords—Arithmetic processor, Digital Chip,MATLAB, Pipeline Array,Simulink.

I. Introduction

Considerable interest has always been shown by various research workers to design new processors with a view to achieve high speed, more memory, less chip area and execution time. Keeping this in view a case study of a pipeline array has been taken up in this paper. A generalized pipeline array published previously [1]−[4] is considered in this paper so as to meet the needs of Cadence technology for MOSIS. The array is also referred in a number of other papers [5]−[8]. The design and VLSI implementation of this array is discussed in a recent reference [4]. It can add subtract, divide, multiply, divide, square and square root binary numbers. In this paper, a case study of a generalized pipeline array is taken up.This processor has 46 pins. The generalized pipeline array has been modelled in Simulink. The objective of the paper is to simulate a model that takes into account the limit of input-output pins for the processor as 40.This is generally accepted by fabrication factories such as MOSIS.

The previous literature has control cells as well as arithmetic cells as shown in Fig. 1 and Fig. 2 respectively. These cells are connected in a specific array format as in Fig. 3. A review of generalized pipeline array is given below as ready reference and for completeness [1]−[4].

As shown in Fig. 1, the arithmetic cell has *A, B, C* as inputs.Line *X* and *F* are control signals. The control cell describes the operations performed and has *P* as input and *F* as output. *Co* passes through adjacent cells as shown in Fig. 2.

The Boolean expressions for arithmetic cell are below:

$$S = [A \oplus (B \oplus X) \oplus C1]\, F + A\bar{F} \quad (1)$$

$$Co = (B \oplus X)\,(A + C1) + AC1 \quad (2)$$

$$D = BC + CF = C\,(B + F) \quad (3)$$

$$E = B + CF = (B + C)\,(B + F) \quad (4)$$

The Boolean expression for control cell is as given below:

$$F = CoX + P\bar{X} \quad (5)$$

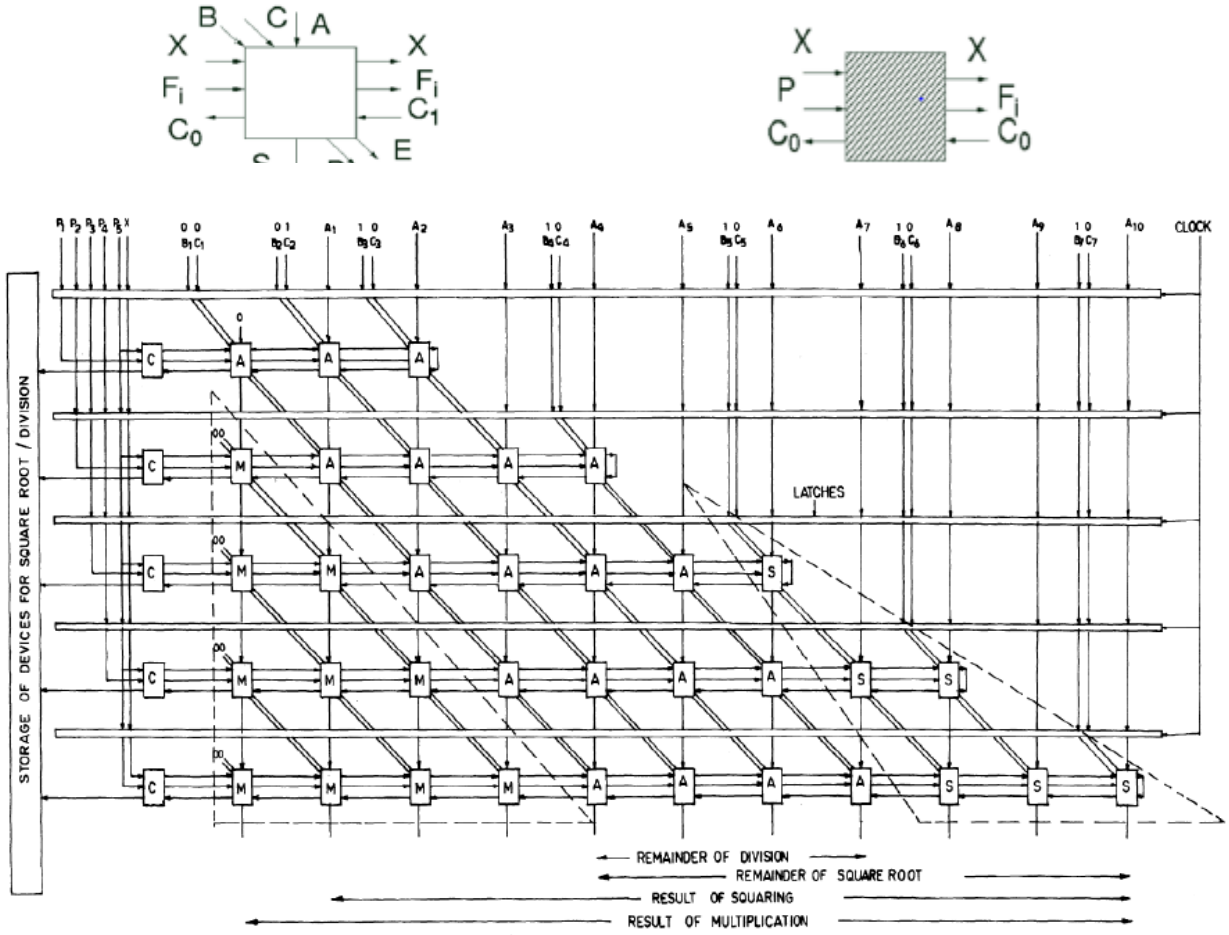

Fig. 3.A generalized pipelinecellular array.

Table I shows number of input/output pins needed for various operations of pipeline array.Please note for all the operations the number of input/output pins required is 46 pins. Table II shows how inputs are assigned to various pins. Please note that for squaring and square rooting *B's* and *C's* are as in array shown in the Fig. 3 above. The*P* bits are assigned left justified for squaring, while right justified for multiplication. The number whose square root is to be found out, is given as N at *A* pins. The dividend for division is given at *B's*. *B* bits are made same as *C* for multiplication and division.

TABLE I
TOTAL INPUT/OUTPUTPINS IN THE PRESENT LITERATURE.

Input Pins						**Output Pins**		**Total**
Operations	***X***	***B***	***C***	***P***	***A***	***F***	***S***	**Sum**
Square	1	7	7	5	10	5	11	46
Square Root	1	7	7	5	10	5	11	46
Multiplication	1	7	7	5	10	5	11	46
Division	1	7	7	5	10	5	11	46

TABLE II
CONDITIONS FOR ARITHMETIC OPERATIONS.

X **value**	**Operation *S***	**Value of *B*&*C***	***P*** **Assignment**	**Value of *A***
0	Squaring	As given in Array	*P*(Left Just)	0
1	Square rooting	As given in Array	0	N
0	Multiplication	*B*=*C*	*P*(right just)	0
1	Division	*B*=*C*	0	D

II. Methodology, Simulation And Chip Development

The main objective of this paper is to design an arithmetic processor with a total number of input/output pins less than 40.One of the MOSIS technologies allows only up to 40 input/output pins. MOSIS is a national science foundation sponsored fabrication facility used by various universities in United States under the educational program. The modified design requires additional circuit. This circuit requires user to determine the operation by giving X and Y values as shown in Table III. This circuit will give the values of C's based on the user input values of X and Y. All values of C's except C2 are AND gates operations between X and B's. The value of C2 is OR gate operation between B2 and the complement of X. From that, in the first two cases were X=0, the values of C's will be as given in array.In the other two operations multiplication and division (when X=1), the values of C's are equal to B's values. By adding this circuit, the total number of pins is reduced to 40. This is one of the requirements of MOSIS fabrication.The circuit is implemented using Simulink is given in Fig. 4. Thedoted rectangular shows the additional circuitry.

This additional circuit is inputted with 2 bitsX and Y which indicate different arithmetic operations, as shown inTableIII. Addition operation is a special case of multiplication and subtraction is a special case of division.

TABLE III
ARITHMETIC OPERATION SELECTION

Pipeline Inputs		**Arithmetic function**
X	***Y***	
0	0	Squaring
0	1	Square rooting
1	0	Multiplication
1	1	Division

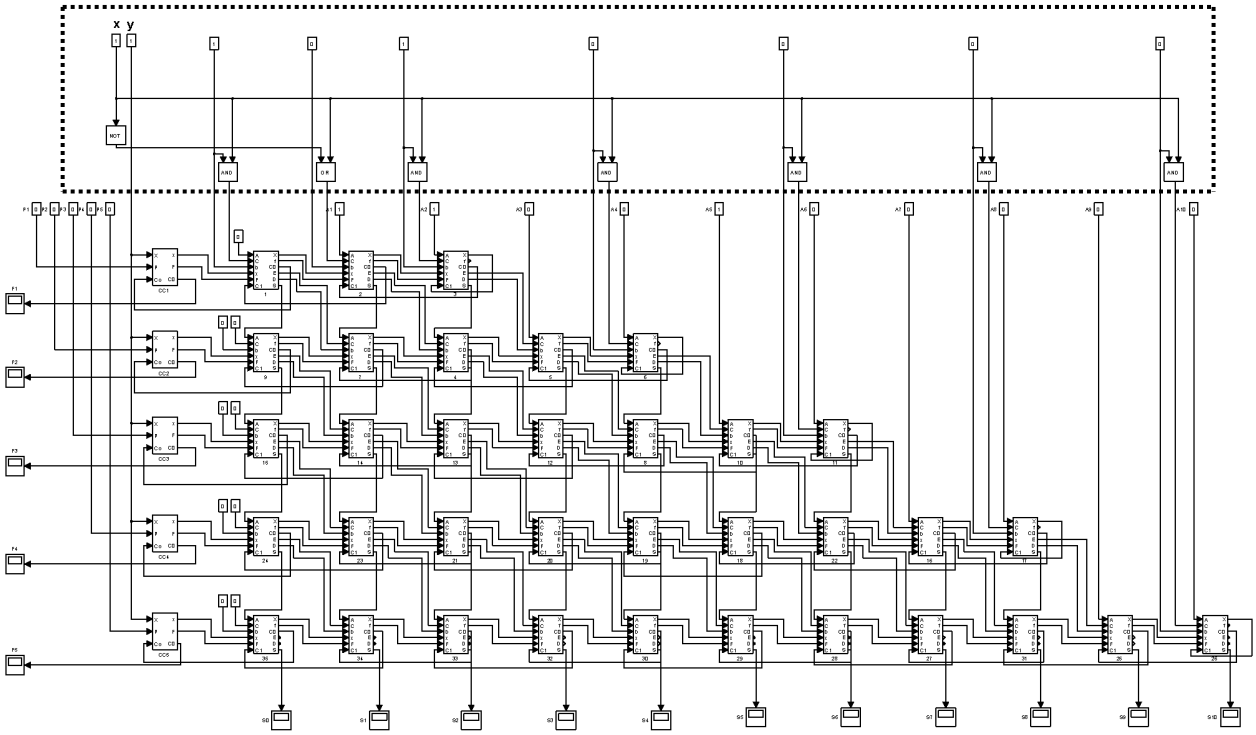

Fig. 4. Pipeline arrayconfiguration.

Table IV gives the number of input-output pins that are used in the present model.

Table V gives the conditions required for different arithmetic operations.

III. RESULTS AND ANALYSIS

Table VI explains the exact values of the pins used for B's, P's, A's for different arithmetic operations and also the exact output pins values for the inputs given. This table shows testing of the following cases. These cases are square of 5, square root of 25, multiplication of 5 and 7, and division of 25 and 5. Fig. 5 shows the total number of pins used is this design. This 40 input/output pins design is suitable for MOSIS fabrication under the educational program of universities.

TABLEIV
NUMBER OF INPUT/OUTPUT PIN FROM PRESENT MODEL

Input Pins						**Output Pins**		**Total**
Operation	***P***	***B***	***C***	**Operation Selection**	***A***	***F***	***S***	**Sum**
Square	5	7	0	2	10	5	11	40
Square Root	5	7	0	2	10	5	11	40
Multiplication	5	7	0	2	10	5	11	40
Division	5	7	0	2	10	5	11	40

TABLE V
MODIFIED CONDITIONS FOR ARITHMETIC OPERATIONS

Arithmetic Operation Selector ***X Y***	**Operation *S***	**Value of *B***	***P* Assignment**	**Value of *A***
00	Squaring	*B1=B2=0,B3=B4…B7=1*	*P*(Left Just)(**Input**)	*A1=A2=….A10=0*
01	Square rooting	*B1=B2=0,B3=B4…B7=1*	*P1=P2=P3=P4=P5=0*	N(**Input**)
10	Multiplication	*B=C*(**Multiplier**)	*P*(right just)**(Multiplicand)**	*A1=A2=….A10=0*
11	Division	*B=C*(**Divisor**)	*P1=P2=P3=P4=P5=0*	D(**Dividend**)

TABLE VI
INPUT/OUTPUT VALUES FROM SIMULATION

Operation Selection	**Operations**	**Value of *B***	***P* assignment**	**Value *A***	**Output *F***	**Output *S***
00	Squaring	*B1=0;B2=0,B3=B4=B5=B6=B7=1*	*P1=1;p3=1,*rest of *P's=0* **(input with decimal value of 5)**	*A1=A2=A3…A10 = 0*	NA	*S2=S3=S6=1,*Rest of *S's=0* **(Result with decimal value of 25)**
01	Square rooting	*B1=0;B2=0,B3=B4=B5=B6=B7=1*	*P1=P2=P3=P4=P5=0*	*A3=A4=A7=1,* Rest of *A's=0* **(Input decimal value of A=25)**	*F1=1;F3=1,* rest of *F's=0* **(Result with decimal value of F=5)**	NA
10	Multiplication	*B2=B3=B4=1,*Rest of *B's=0* **(Multiplier with a decimal value of 7)**	*P5=1;P3=1,* rest of*P's=0* **(decimal value of 5)**	*A1=A2=A3…A10 = 0*	NA	*S2=S6=S7=1,* rest of *S's=0* **(decimal value of 35)**
11	Division	*B1=B3=1,* Rest of *B's=0* **(Dividend with a decimal value of 5)**	*P1=P2=P3=P4=P5=0*	*A1=A2=A5=1,* Rest of *A's=0* **(divisor with a decimal value of 25)**	*F2=F4=1,* rest of *F's=0* **(Result with decimal value of 5)**	NA

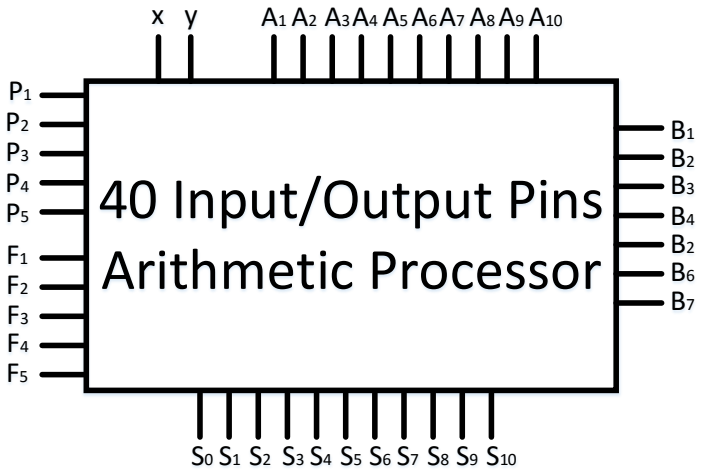

Fig. 5.Simplified diagram for showing number of pins used for the design

IV.CONCLUSION

There will always be interest in the development of new arithmetic processors and their VLSI implementation to get a fabricated chip .With this objective a case study of a generalized pipeline array has been taken up in this paper. Thereare different approachesin the design and development of arithmetic processor. The generalized pipeline cellular array exploits a cellular type of approach as compared to other conventional approaches which require the design of registers etc.Moreover, the array approach discussed here utilizes hardware design of the basic operations such as addition, subtraction, division, squaring and square rooting.The design of arithmetic circuit using hardware implementation has been taken up in this work. The design developed here meets the 40 input/output pins requirements as needed by one of the MOSIS fabrication technology .The design has been simulated using simulink and tested for various operations given in the paper. The test results are shown in Table VI. It is hoped such an approach for the design of arithmetic processor and VLSI implementation of such design into chip will help in the future designs of processors in general and arithmetic units in particular. More work is also needed to extend such designs to higher number of bits such as 1 byte and 2 bytes operations.

References

[1] A. K. Kamal, H. Singh, D. P. Agrawal, "A generalized pipeline array,"*IEEE Transactions on Computers* , vol.C-23, no.5, pp.533-536, May 1974.

[2] Kai Hwang, "Computer Architecture: Principles, Architecture And Design", ISBN: 0471052000, 1979, John Wiley & Sons Inc, US.

[3] Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", McGraw-Hill Book Co., NY, april 1993. Chinese translation by Tsinghua University Press, China, August 1995.

[4] Harpreet Singh et al., "On simulation and design implementation of generalized pipeline cellular array ," in *Int. Conf. on Inform. Sci., Electron. and Elect. Eng. (ISEEE)*, Sapporo, Apr. 2014, pp. 1761-1765.

[5] Peter M. Kogge, "*The Architecture of Pipelined Computers*", CRC Press, 1981.

[6] Kai Hwang, *Computer Arithmetic: Principles, Architecture and Design*. Hoboken, NJ: John Wiley & Sons, Apr. 1979.

[7] Peter M. Kogge, *The Architecture of Pipelined Computers*. Boca Raton, FL: CRC Press, Jan. 1981.

[8] Agrawal, Dharma P., "High-speed arithmetic arrays," *IEEE Trans. Comput.*, vol. 28, pp. 215-224, Mar. 1979.