Comparison of Temperature Dependent Performance and Analysis of SWCNT bundle and Copper as VLSI Interconnects

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Abstract

This paper presents the analysis and the performance of Single Walled Carbon Nanotube (SWCNT) bundle as VLSI interconnects by considering the effect of temperature for different technology nodes. An equivalent temperature dependent RLC circuit model presented and comprehensive analysis of delay and power is done for 32nm, 22nm and 16nm technology nodes for both SWCNT bundle interconnects and copper interconnects. It is revealed form the results that SWCNT bundle interconnects offers smaller value of resistances and it due to its longer mean free path (MFP) of SWCNT as compare to copper interconnects. On the basis of impedance parameters, simulation results are also present which show that the densely packed SWCNT bundle interconnects can easily be replaced with its counterpart copper interconnects for global interconnects. Hence SWCNT bundle interconnects is a promising alternative to copper as VLSI interconnect for advanced technology nodes.

Keywords: Interconnects, Technology nodes, Single-walled Carbon nanotubes (SWCNT), Very Large Scale Integration (VLSI), Temperature dependency.

1. Introduction

An Interconnect is used to provide electrical connections between different nodes of the electrical circuit. Copper (Cu) was widely used material as interconnect due to its good conductivity and high current density [1]. Due to advancement in VLSI technology, a number of problems like surface roughness, grain boundary scattering, Electro-migration, causes to sharply increase in propagation delay and power dissipation for copper interconnects. [2] and [3]. So to improve these problems alternative materials have been considered.

Carbon nanotubes (CNT) have the potential to replace the copper as interconnects due to its advantages. CNT has several micrometer long electron mean free path (MFP) as compared to copper which has a few tens of nm mean free path [3].

CNTs are known as allotrope of carbon and made by rolling up a sheet of graphene sheet into a cylinder. As per its structures, a single-walled CNT (SWCNT) consists of one rolled up graphene sheet whereas multi-walled CNT (MWCNT) consists more than two rolled up graphene sheets with diameter ranging from few nanometer to several tens of nanometer [4] and [5]. SWCNTs are hollow cylinders formed by only one thin wall of graphene with diameters ranging from 1-2nm [6].These can be either metallic or semiconducting depends. Metallic SWCNTs are used an interconnect material because of good thermal and mechanical stability. An individual SWCNT with small diameter (1nm-2nm) has high resistance and to reduce the resistance, SWCNT

bundles are used as interconnects which consists of large number of isolated SWCNTs in parallel as shown in Fig1 [7] and [8].

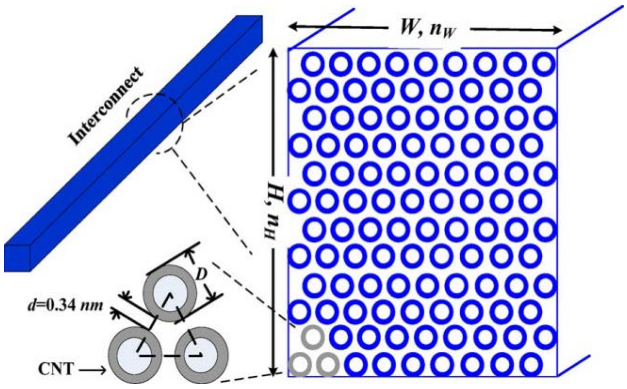


Fig.1:Cross-sectional view of a SWCNT bundle with width W and height H. The diameter of each SWCNT is D, and the interval between two adjacent SWCNTs is d. n_W and n_H are the numbers of SWCNTs along the width and height, respectively[8].

While SWCNTs have desirable material properties, individual nanotubes suffer from an intrinsic quantum resistance of 6.45kΩ (approx). As a result, the resistances of isolated SWCNTs causes excessive delay for interconnect applications. The intrinsic resistance problem is solved by considering bundles of SWCNTs in parallel [6].Thus, their small dimension and ability to operate at wide bias range are well suited for interconnect applications. Before such applications can be implemented into electronic devices, much still needs to be understood about the electrical properties of SWCNTs.

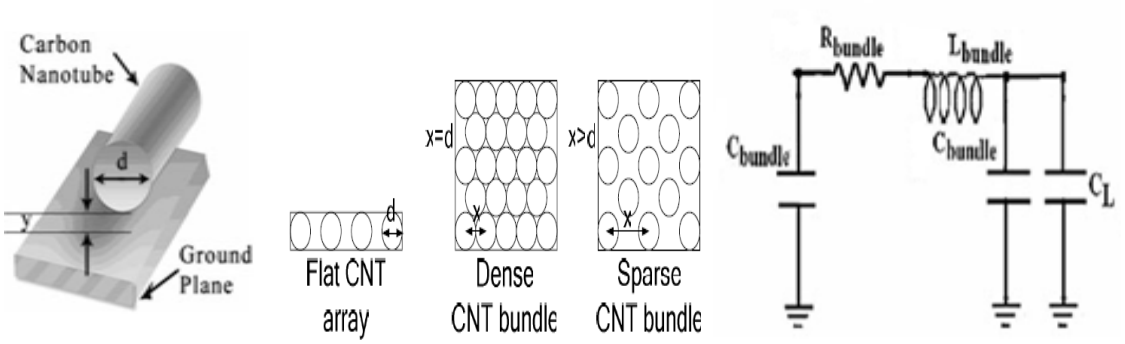
For high performance ICs for its different application has great variance in the temperature (200K-450K). These temperature variations may affect the performance of SWCNT based interconnects in terms of delay and power dissipation. Due to temperature variations, there is significant effect on the electron surface and grain boundary scattering mechanism in SWCNT [9] and [10].This scattering mechanism reduces the mean free path of the SWCNT and due to which the impedance parameters of SWCNT get affected. These temperature dependent impedance parameters have significance effect on the performance SWCNT in terms of delay and power. This paper includes the influence of temperature and size on the electrical performance of SWCNT bundle interconnects and copper interconnects. These two parameters effect electrical performance of these interconnects [11] and [12]. The effect of temperature has been studied and reported in this paper for global interconnects at 32nm, 22nm and 16nm technology nodes.

The section 2 of the paper presents the temperature dependent model of SWCNT bundle interconnects and section 3 introduces the temperature dependent model for copper interconnects. In section 4, the simulated results for 32nm. 22nm and 16nm in terms of delay and power are compared for SWCNT bundle interconnects and copper interconnects at temperature ranging from 200K-450K for global interconnects length (~1mm). Finally it is concluded in

section 5 that SWCNT bundle shows better performance than its counterpart and can be successfully used as an alternative as interconnect for advanced technology node for moderate to high temperature range.

2. Temperature dependent impedance model for SWCNT Bundle Interconnects

An individual SWCNT shell with small diameter has equivalent to RLC circuit which consists of diameter, length and temperature dependent resistance, inductance and capacitance [5] and [8]. A schematic of an individual shell of SWCNT on ground plane is shown in Fig.2a. An isolated SWCNT shell with diameter *d* is separated from ground plane with distance *y*. The parallel combination of such individual SWCNT shells forms a SWCNT bundle for VLSI interconnects as shown in Fig. 2b. [5]. The equivalent circuit model of SWCNT bundle to a tandem of such RLC circuits is shown in Fig.2c.



(a) (b) (c)

Fig.2. Schematic and equivalent circuit of SWCNT. Fig.2a. shows individual SWCNT shell on ground plane. Fig.2b. shows SWCNT bundle with separation distance of two adjacent individual shells and Fig2.c. shows the temperature dependent equivalent RLC model for SWCNT bundle interconnects[5] and [9].

2.1. R, L, and C of an Individual Shell of SWCNT bundle

The temperature dependent individual shell of metallic SWCNT discussed on the basis of its electrical equivalent circuit. Depending on different interconnect parasitic such as resistance, capacitance and inductance, the impedance model of an individual shell for metallic SWCNT is shown in Fig.3 [12] .

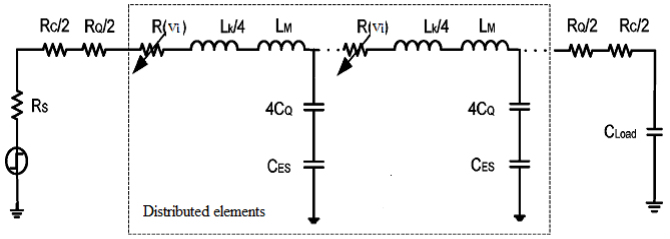


Fig.3. Equivalent circuit model of an individual shell of metallic SWCNT [12]

The equivalent resistance of an individual of metallic SWCNT shell can be divided into three resistive components [8] which are electron-phonon based scattering-induced resistance R_S (considered only when the length of nanotube is larger than its MFP), quantum resistance R_Q, and imperfect metal contact resistance $R_{mc..}$ The imperfect contact resistance mainly depends upon the metal used for contacting with CNT and can range from zero to hundred of kilo-ohm for different growing processes [10]. It is almost independent from the diameter and temperature. Therefore the value for the contact resistance is almost constant and assumed 24kΩ for each shell of SWCNT bundle as suggested in [9]. Hence the temperature dependent shell resistance [9] is given by

$$R_{shell} = R_Q + R_S.L = \frac{h}{2e^2 N(T)} + \frac{h}{2e^2 N(T)}.\frac{L}{\lambda eff\,(T)} \qquad (1)$$

Where $h/2e^2$= 12.9kΩ, L, $\lambda_{eff}(T)$ and $N(T)$ are the length, temperature dependent effective mean free path (MFP) and number of conducting channels of an individual shell respectively. It is observed from equation (1) that the effective MFP play an important role in determining the value of resistance of the shell and MFP of nanotube is depends upon scattering mechanism of electron and phonon [9], [11] and [12].

The electron-phonon scattering mechanism is the major source of scattering where the role of electron-electron scattering mechanism is negligible small for SWCNT [9].The acoustic scattering phenomena and optical zone boundary scattering phenomena are two components of the scattering phenomena of electron-phonon scattering of SWCNT. Therefore, scattering dependent MFP (λ_{eff}) can be given as

$$\lambda_{eff} = \left[\frac{\lambda_{AC}.\lambda_{OZB}}{\lambda_{AC} + \lambda_{OZB}}\right] \qquad (2)$$

Where λ_{AC} is acoustic MFP (due to acoustic scattering phenomena) and λ_{OZB} is optical and zone boundary MFP (due to optical and zone-boundary scattering phenomena) [9]. The resistance of SWCNT at low to moderate temperature, by and large depends upon the acoustic phonon scattering MFP (λ_{AC}) [10].The acoustic MFP (λ_{AC}) is directly depends upon the temperature and diameter of SWCNT and can be given as

$$\lambda_{AC}(T) = 890\frac{T_0 D_i}{T} \qquad (3)$$

Where T_0=300K, T is temperature in Kelvin and D_i is diameter for isolated shell of SWCNT [8] and [9]. It is observed from the equation (3) that with increase in temperature, the acoustic MFP (λ_{AC}) decreases. For moderate to high temperature the optical and zone boundary MFP (λ_{OZB}) also play a comparable role at low bias. In case of high bias condition, the electric field generated along the CNT accelerates the electrons and increases their kinetic energy. When the electron energy reaches the optical phonon energy level, a phonon will be emitted with energy

hω (hω ~ 0.16eV in case of zone-boundary phonon and hω ~ 0.2 eV in case of optical phonon) [9], [10] and [12]. Optical or zone-boundary scattering can take place when an electron acquires the required energy by absorbing another optical or zone-boundary phonon, respectively Therefore, λ_{OZB} can be written as

$$\lambda_{ozB} = \left[\frac{\lambda_{ozB,\,fld} . \lambda_{ozB,abs}}{\lambda_{ozB,\,fld} + \lambda_{ozB,abs}} \right] \tag{4}$$

where $\lambda_{ozB,fld}$ is the MFP due to the electric-field acceleration based scattering and can be represented as

$$\lambda_{OZB,\,fld} = \frac{(h\omega - k_B T)}{eV} L + \frac{\lambda_{ozB,300} D_i}{D_o} \frac{N_{ozB}(300)+1}{N_{ozB}(T)+1} \tag{5}$$

where k_BT is the thermal energy (k_B is the Boltzmann's constant). The first term correspond to the distance that the electron must travel to reach the phonon emission threshold energy, and the second term represents the distance that the electron travels after gaining the energy before emitting the phonon. λ_{OZB300}~15nm is the measured spontaneous effective emission length for diameter D_0 at 300 K [9]. N_{OZB} =1/[exp(hω/k_BT)-1] is the optical or zone-boundary phonon occupied states [9] and [13]. $\lambda_{OZB,abc}$ measures the scattering effect due to absorbing an optical or zone-boundary phonon and can be written as

$$\lambda_{ozB,abs} = \frac{\lambda_{ozB,300} D_i}{D_o} \frac{N_{ozB}(300)+1}{N_{ozB}(T)} \tag{6}$$

All the individual SWCNT tubes of a bundle are considered to be parallel to each other and hence the total resistance of the bundle is depending upon the size of the bundle. The total temperature dependent resistance (R_{Bundle}) of bundle SWCNT with length L, temperature dependent mean free path (λ_{eff}) is considered as all individual shells of SWCNT as parallel and given by equation (7) [14],[15] and [16].

$$R_{(Bundle)} = \frac{R_{shell} + R_{mc}}{n_{bundle}}$$

$$R_{(Bundle)} = \frac{\frac{h}{2e^2 N(T)} + \frac{h}{2e^2 N(T)} . \frac{L}{\lambda eff\,(T)} + R_{mc}}{n_{Bundle}} \tag{7}$$

Where N and n_{Bundle} are number of conducting channels and number of SWCNT tubes in a SWCNT bundle [17]. The total number of SWCNT tubes (n_{Bundle}) in a bundle is given by equation (8), where *d* is tube diameter, *H* is height and *W* is width of bundle interconnects as shown in Fig.2b [5].

$$n_{Bundle} = \left[\frac{W-d}{x}\right]\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor+1\right)-\frac{1}{2}\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor+1\right) \quad (8)$$

If the number of rows in the bundle is even and

$$n_{Bundle} = \left[\frac{W-d}{x}\right]\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor+1\right)-\frac{1}{2}\left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor\right) \quad (9)$$

If number of rows are odd. Where the number of rows depend upon *x*, which is center to center distance of adjoining tubes of bundle as shown in Fig.2b and given by

$$n_{H(Bundle)} = \left(\left\lfloor\frac{H-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right\rfloor+1\right) \quad (10)$$

The inductance of SWCNT bundle is also considered as parallel combination of inductance offered by individual SWCNT and given by

$$L_{(Bundle)} = \left(\frac{L_M + L_K}{4n_{Bundle}}\right) \quad (11)$$

Where L_M and L_K are the magnetic and kinetic inductances of an individual SWCNT and are calculated by using equation (12) and (13).

$$L_{magnetic} = \left(\frac{\mu}{2\pi}\right).cosh^{-1}\left(\frac{2h_t}{D_i}\right) \quad (12)$$

$$L_{K/channel} = \frac{h}{2\times 2v_f e^2} \approx 8nH/\mu m \quad (13)$$

The total capacitance of SWCNT bundle is given by equation (14), which consists of bundle electrostatic capacitance and bundle quantum capacitance of SWCNT and can be given by equation (15) and (16) [5] and [6]

$$C_{(Bundle)} = \left(\frac{C_E^{Bundle} . C_Q^{Bundle}}{C_E^{Bundle} + {}_Q^{Bundle}} \right) \quad (14)$$

$$C_E^{(Bundle)} = 2\left(\frac{2\pi\varepsilon_{ox}}{\ln(s/d)} \right) + \left(\frac{W-d-2}{2} \right) \left(\frac{2\pi\varepsilon_{ox}}{\ln(\frac{s+W}{d})} \right) + 3\left(\frac{2\pi\varepsilon_{ox}}{\ln(s/d)} \right) \left(\frac{{}^{n}H(bundle)-2}{5} \right) \quad (15)$$

$$C_Q^{Bundle} = \left(\frac{2\times 2e^2}{hv_f} \right) n_{CNT} \quad (16)$$

3. Temperature dependent impedance model for copper

The analysis of temperature dependent copper interconnects is done in this section. The schematic set up used to calculate equivalent temperature dependent impedance parameters for a copper interconnect is shown in Fig.4 [18] and [19]. Fig. 4 shows, the cross-section view of copper interconnects with width 'W', thickness 't', height 'h' from ground and separation 's' between two adjacent interconnects.

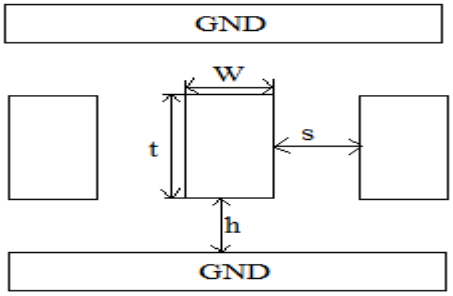


Fig.4. Interconnect geometry for copper interconnects [13]

3.1.Resistance

The resistance per unit length of copper interconnect [12] with rectangular cross-sections strongly depends upon the resistivity as given below

$$R_{Cu} = \frac{\rho(T)L}{W\,t} = \frac{\rho_s + \rho_d}{W\,t} L \quad (17)$$

ρ(T) is resistivity of copper interconnect. The resistivity ρ is the strongly depends upon temperature and may be separated into two parts. The temperature dependent part of resistivity is due to phonon surface scattering (ρ_s)and temperature independents part is related to defect (ρ_d).[11] and [19]

$$\rho(T) = \rho_s(T) + \rho_d \quad (18)$$

$$\rho(T) = \rho_0\left[1 + 0.00401(T - T_0)\right] \quad (19)$$

where ρ_0 is technology dependent resistivity of copper at 300K and value for different technology nodes is given in table 1 [13] and T_0 =300K.

3.2.Inductance

The inductance of copper interconnects with a rectangular cross-section area can be expressed [11] and [12] as

$$L_{Cu} = \frac{\mu_0 L}{2\pi}\left[\ln\left(\frac{2L}{W+t}\right) + \frac{1}{2} + \frac{0.22(W+t)}{L}\right] \quad (20)$$

Where μ_0 is the permeability and its value is given as $4\pi \times 10^{-7}$H/m.

3.3. Capacitance

The capacitance C_g of the copper interconnect is the capacitance of area and fringe flux to the underlying plane and expressed as [12]

$$C_g = \varepsilon\left[\frac{W}{h} + 2.22\left(\frac{s}{s+0.7h}\right)^{3.19} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76} \cdot \left(\frac{t}{t+4.53h}\right)^{0.12}\right] \quad (21)$$

Where C_g is capacitance of per unit length, W, h, t are width, height and thickness copper interconnects and s is separation between two interconnects as per interconnects geometry shown in Fig. 4. ε is dielectric constant for copper interconnect and it is technology dependent and given in table 1.

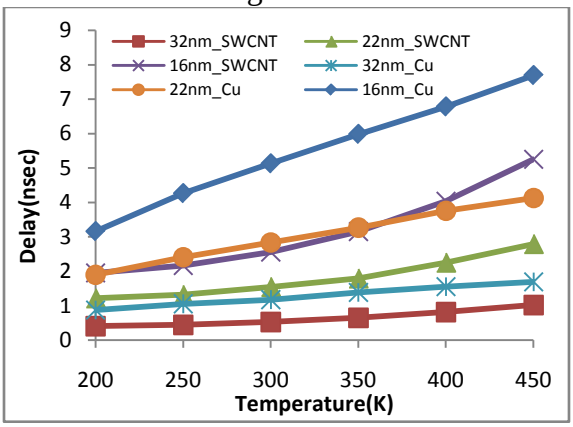
Table 1: ITRS 2005 based Simulation Parameters for global interconnect [13], [20] and [21]

Technology Node	32nm	22nm	16nm
Width W(nm)	48	32	21
Thickness H (nm)	144	96	43
Aspect Ratio(A/R)	3	3	3
Oxide thickness t_{ox}(nm)	110.4	76.8	52.5
V_{DD} (volts)	0.9	0.8	0.7
Dielectric constant (ε)	2.25	2.05	1.75
$D_{ratio}(D_{min}/D_{max})$	0.5	0.5	0.5
ρ_o for Cu(μΩ.cm)	3.52	4.2	5.38
PTM model file [21]	54	54	54
Interconnects length(mm)	1	1	1

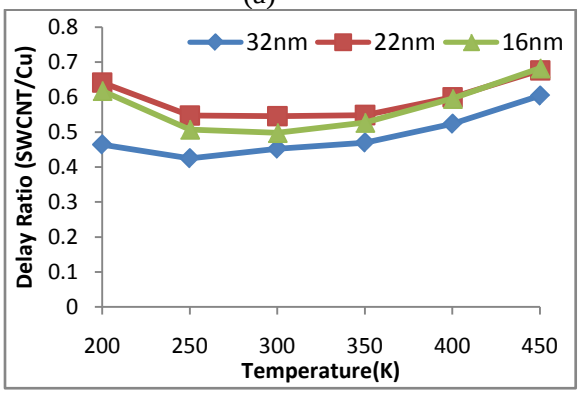
Load Capacitance (fF)	10	10	10
Frequency (GHz)	1	1	1

4. RESULTS AND DISCUSSIONS

The temperature dependent impedance parameters are calculated for SWCNT bundle interconnects using the equations 1 to 16 and for copper interconnects using 17 to 21 respectively, for temperature ranging from 200K to 450K at 32nm, 22nm and 16nm technology nodes for 1mm interconnect length. The temperature dependent calculated values of resistance, capacitance and inductance are simulated using PSPICE tools for all three technology nodes [22] and [23]. All interconnect parameters used for calculations and simulations are obtained from ITRS 2005 [13], [20] and [21], as summarized in table 1. Fig. 5 shows the results in terms of delay for different technology nodes at temperature ranging from 200K to 450K. From the results it revealed that as temperature increases the delay is increases for all the technology nodes and this decrease is due to decrease in the mean free path. It is also found that the delay of SWCNT interconnects is smaller than that of copper interconnects and the improvement in delay performance in the case of SWCNT interconnects is increases than the copper interconnects with rise in temperature at global interconnects length.



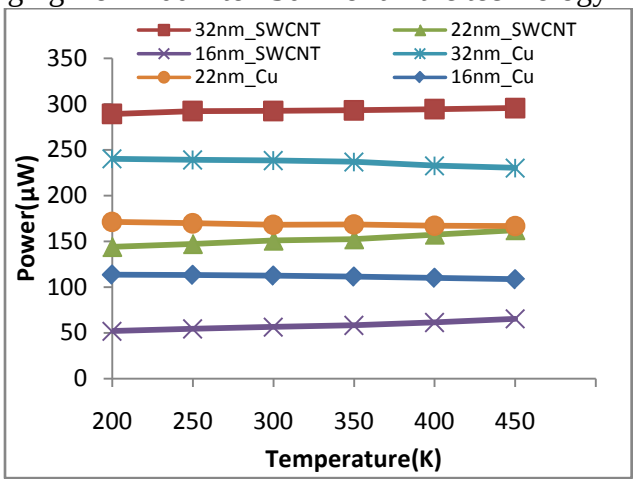
(a)



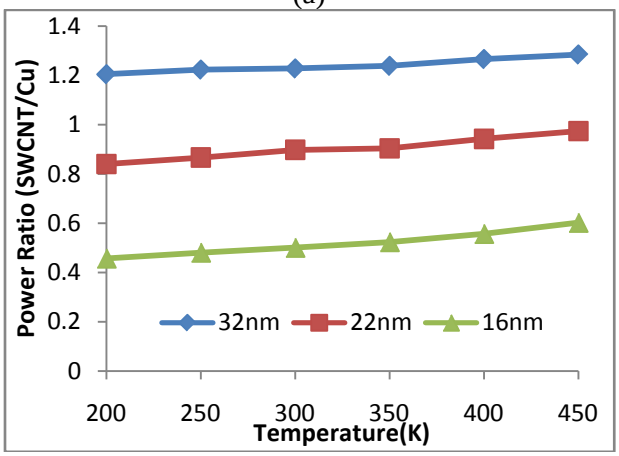
(b)

Fig. 5 (a).Comparison of the performance of SWCNT bundle Interconnect and copper interconnects for 32nm, 22nm and 16nm technology nodes and (b). Shows comparison of PDP ratio of SWCNT bundle to copper interconnects

Fig.5. (b) shows the relative delay ratio of SWCNT bundle and copper interconnects for temperature range 200K to 450K at different technology nodes (32nm, 22nm and 16nm). The results revealed that the delay ratio for all three technology nodes is less than unity and hence it is concluded that the performance of SWCNT is better than that of copper interconnects at variable temperature ranging from 200K to 450K for all the technology nodes.



(a)

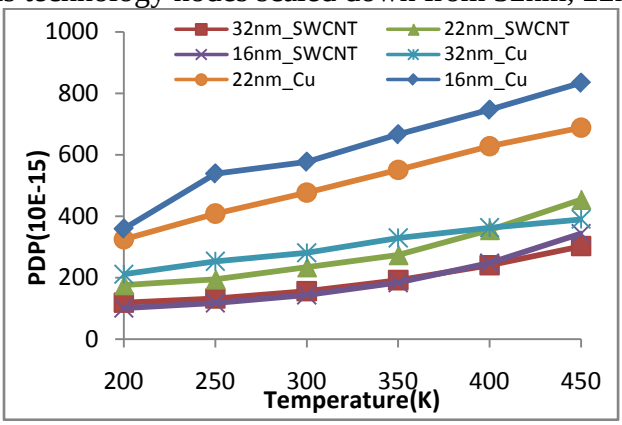


(b)

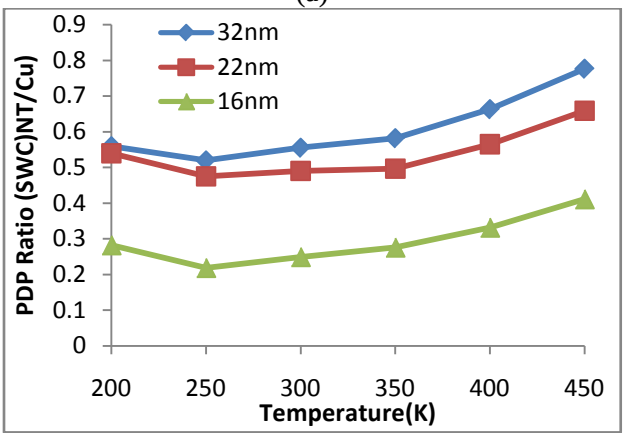
Fig.6. (a) Comparison of performance of copper and SWCNT bundle interconnect in terms of power for 1000µm interconnect length at 32nm, 22nm and 16nm technology nodes. (b) Comparison of performance of copper and SWCNT bundle interconnect in terms of relative power ratio (SWCNT/Cu).

Fig.6.(a) shows the comparison of power dissipation of SWCNT bundle and copper interconnect for three different technology nodes at temperature ranging from 200K to 450K. It is revealed from the results that SWCNT has more power dissipation than copper because of higher capacitance in case of SWCNT bundle compared to copper interconnects. This analysis is done at 1000µm length of interconnect at maximum attainable frequency at 1 GHz for 32nm, 22nm

and 16nm technology nodes. It is also concluded from Fig.6(b) that the power ratio (SWCNT/Cu) reduces as technology nodes scaled down from 32nm, 22nm to 16nm.



(a)



(b)

Fig.7. (a) Comparison of performance of SWCNT bundle and copper interconnects in terms of power delay product (PDP) for 1000µm interconnect length at 32nm, 22nm and 16nm technology nodes respectively. (b) Comparison of performance of MWCNT bundle and SWCNT bundle interconnects in terms of relative PDP ratio (MWCNT/SWCNT).

Fig.7 (a) and (b) show the performance in terms of PDP of SWCNT bundle and copper interconnects for 32nm, 22nm and 16nm technology nodes for temperature ranging from 200K to 450K. Power delay product (PDP) of an interconnect decides whether it has potential of being a reliable interconnect for the given technology. It is discovered from the results that the power delay product of SWCNT bundle and copper interconnects increases with increase in temperature at different technologies since both power and signal delay increases with increase in temperature. It is also concluded that the performance in terms of PDP is improved with scaled down technology

5. CONCLUSION

The thermal conductivity for SWCNT bundle interconnects and copper interconnects is determined for variable temperature ranging from 200K to 450K at 32nm, 22nm and 16nm

technology nodes. The signal delay and power calculations show that increase in temperature across SWCNT bundle interconnect and copper interconnects increases. This increase in delay and power due to increased in electron–phonon scattering. It is also concluded that the delay offered by SWCNT bundle interconnects is very less as compare to the copper interconnects. Further, the decrease in power delay product (PDP) with scaled down technology nodes shows that SWCNT bundle interconnects is a suitable candidate for future VLSI applications at scaled down technologies nodes for moderate to high temperature range. It is also concluded SWCNT bundle interconnects show the better performance in all aspest than its counterpart and can be successfully used as an alternative as interconnect for advanced technology node for moderate to high temperature range.

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