A Genetic Algorithm for ordering and reduction of BDDs using Crossover Operators for MIMO VLSI Circuits

[1]Manu Bansal, [2]Alpana Agarwal
[1,2]Department of Electronics and Communication Engineering
Thapar University, Patiala, India.
[1]mbansal@thapar.edu, [2]alpana@thapar.edu

Abstract—This paper proposes genetic algorithm with three crossover operators namely order, cycle and partially mapped (PMX) for minimization of shared ordered BDDs .The results obtained with the above said three crossover operators have been compared with the existing algorithms in the literature for LGSynth93 Benchmark Circuits and Multi-input Adders. For multi- input and multi-output circuits the reduction in number of node count is tremendous. As inputs keep on increasing the reduction in node count keeps on increasing. For 5xp1 benchmark circuit the reduction is about 22.7%, whereas for b12 benchmark circuit the reduction is about 34%, for squar5 benchmark circuit the node count reduction is about 2.6% and for pdc benchmark circuit it is about 9.4%. For 1-bit and 2-bit adders, crossover reduction in node count is about 0%, for 3-bit adder it is about 18.75%, for 4-bit adder it is about 44.44%, 5-bit adder shows about 65.07% reduction, 6-bit adder has about 77.07%, 7-bit adder has about 85.82% and for 8-adder is about 74%. Therefore, the proposed Genetic algorithm is suitable for multi-input multi-output (MIMO) VLSI circuits.

Keywords : Genetic Algorithm, Optimization, Variable Ordering, BDDs, Order, Cycle, Partially Mapped.

1. INTRODUCTION

Binary Decision Diagrams (BDDs) [1-3] are the data structures that are used for compact representation of Boolean functions. BDD is a finite directed acyclic graph (DAG) with a unique initial node as shown in figure 1. Every non-terminal node is marked by a Boolean variable. There are exactly two edges, labelled 0 and 1, from one non terminal node to other nodes. Shannon decomposition is carried out for each node. The need of the time is that we need to optimize chip area usage to increase its functionality. A good variable order is needed that minimizes the size. In this paper, genetic algorithm with three versions of the crossover operator has been used for BDD minimization: Order Crossover, Partially Mapped Crossover and Cycle Crossover.

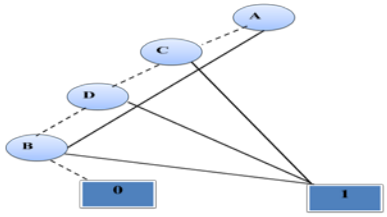

Fig1 Binary Decision Diagram for the function F=AB + A'C + BC'D

2. GENETIC ALGORITHM FOR BDD REDUCTION

Genetic Algorithms GA, [4, 10] are a family of excellent optimization techniques based on Darwinian Theory. The objective of GA is to find an optimal ordering of BDDs with reduced node count and computation time. GAs work by finding a best individual i.e. BDD ordering from a population of individuals evolved over many generations. A fitness value *i.e.* in terms of node count is assigned to each individual *i.e.* BDD order. A population of random individuals is initialized. Parents are selected based on their fitness values and crossover and mutation operations are performed on them to generate offspring with a better fitness value i.e. node count. The process is continued till an optimum solution i.e. BDD with least node count is found.

3. CROSSOVER OPERATORS FOR GENETIC ALGORITHM

Crossover [5] is an important step in the genetic algorithm. The crossover operator strongly affects the performance of genetic algorithm. Three versions of the crossover operator have been used for BDD minimization:

3.1. **Order Crossover**: The elements on left hand side of crossover point of parent 1 are directly copied to offspring at same positions. The remaining fields of the offspring are filled by the elements of parent 2 in order.

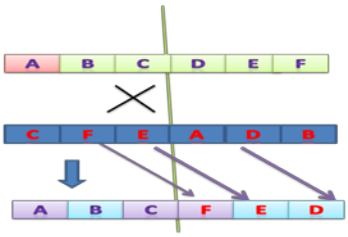

Fig2 Order Crossover

3.2. **Partially Mapped Crossover**: Cells on right hand side of the crossover point in both parents are partially mapped.

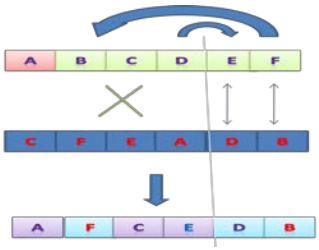

Fig3 PMX Crossover

3.3. **Cycle Crossover:** Every cell in offspring occupies position similar to either of the two parents.

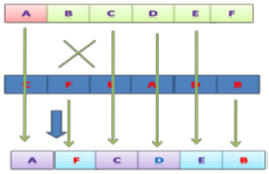

Fig4 Cycle Crossover

4. PROPOSED ALGORITHM/ FLOWCHART for BDD MINIMIZATION

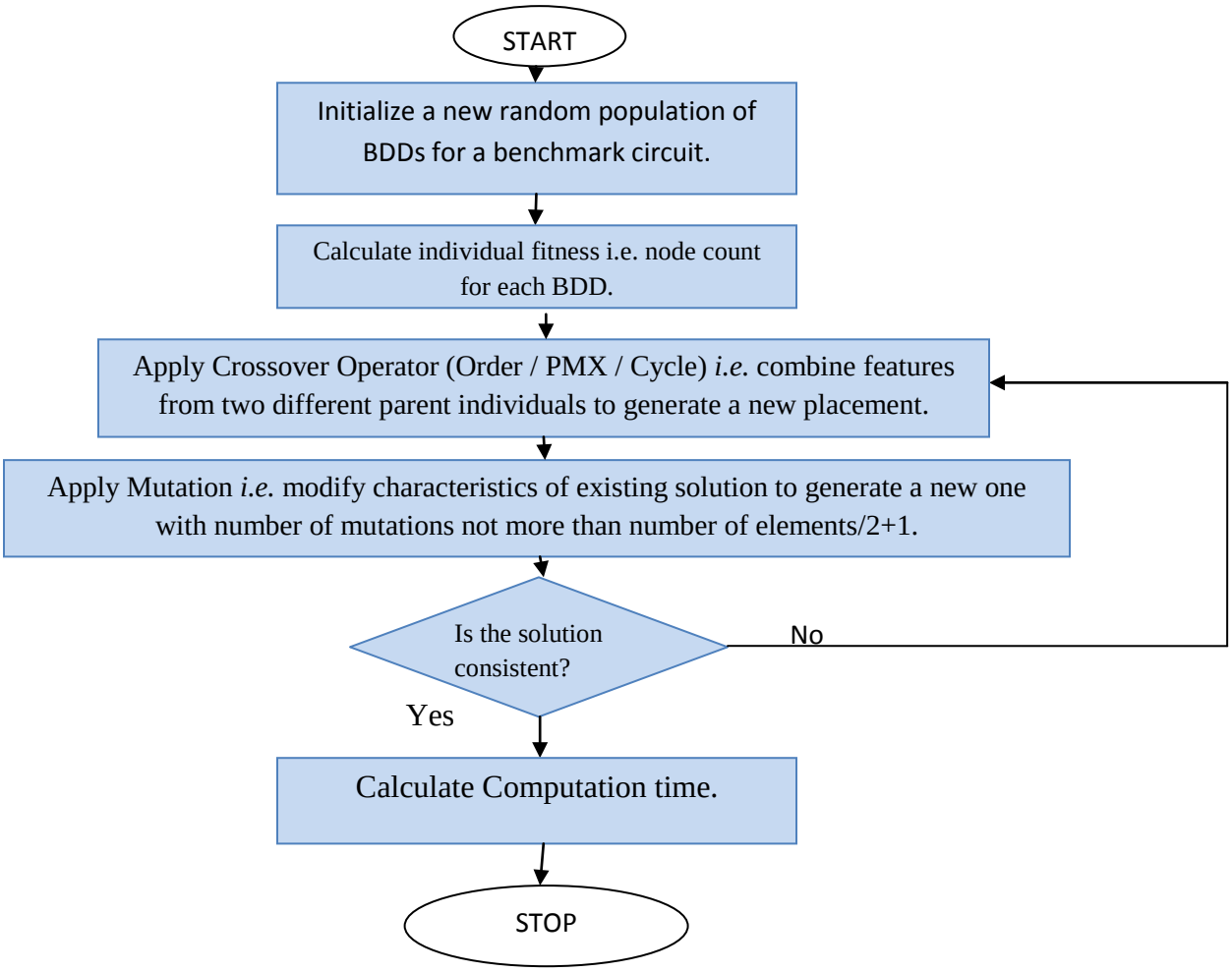

Fig5 Proposed Flow-chart for using Genetic Algorithm

5. SIMULATION RESULTS

The Proposed Genetic algorithm, using three types of crossover operators, is implemented with C++ codes and simulated using BUDDY 2.4 package on Ubuntu 12.04. In this section, simulation results *i.e.* node count for LGSynth93 benchmark circuits and Multi-input Adders has been presented in Table I and II.

6. CONCLUSIONS

It is observed that in comparison with other existing algorithms, The proposed GA technique gives minimum node count. Also, when the operators are compared, Partially Mapped Crossover gives minimum nodes, e for most of the circuits. The order crossover also gives optimum results. Table1 shows that the node count for multi-input and single-output circuits i.e. xor5 benchmark circuit and t481 benchmark circuit is same for all the existing as well as proposed algorithm. For multi- input and multi-output circuits the reduction number of node count is tremendous. As inputs keep on increasing the reduction in node count keeps on increasing. For 5xp1 benchmark circuit the reduction is about 22.7%, b12 benchmark circuit is about 34%. For multi- input and multi-output circuits where the number of outputs are equal or more than the number of inputs, the reduction in the node count is not considerable. For squar5 benchmark circuit the node count reduction is about 2.6%, pdc benchmark circuit is about 9.4%. In multi-input adder circuits, as number of inputs are increasing, the proposed genetic algorithm with PMX crossover gives best reduction in node count. From Table II, for 1-adder, with crossover reduction in node count is about 0%, for 2-adder is about 0%, for 3-adder is about 18.75%, for 4-adder is about 44.44%, for 5-adder is about 65.07%, for 6-adder is about 77.07%, for 7-adder is about 85.82% and for 8-adder is about 74%. Therefore, the proposed Genetic algorithm is suitable for multi-input multi-output (MIMO) VLSI circuits.

Table I Comparison of Node Count for Dynamic and Genetic algorithms for LGSynth93 Benchmark Circuits.

SNo.	Benchmark Circuits	Inputs	Outputs	Initial Node Count	WIN2	WIN2ite	WIN3	SIFT	RANDOM	Proposed GA with Crossover		
										ORDER	CYCLE	PMX
1	xor5	5	1	9	9	9	9	9	9	9	9	9
2	con1	7	2	18	20	18	16	18	18	15	16	15
3	t481	16	1	32	32	32	32	32	74	32	89	32
4	squar5	5	8	38	38	38	38	38	38	37	37	37
5	sqrt8	8	4	42	40	39	37	37	48	33	34	33
6	misex1	8	7	47	43	42	41	41	47	37	37	36
7	inc	7	9	81	83	80	74	73	86	72	72	72
8	5xp1	7	10	88	87	82	82	82	88	68	68	68

9	b12	15	9	91	86	86	65	65	76	66	68	60
10	misex2	25	18	99	140	126	111	86	83	105	122	89
11	clip	9	5	105	254	178	108	105	105	107	157	94
12	bw	5	28	118	113	112	106	106	118	106	106	106
13	sao2	10	4	154	149	109	91	92	132	90	92	85
14	Pdc	16	40	696	666	658	640	640	709	665	696	630
15	misex3c	14	14	750	719	490	454	527	844	549	680	469
16	table5	17	15	873	776	738	717	712	974	826	926	740
17	duke2	22	29	976	825	777	360	358	414	452	537	364

Table II Comparison of Node Count for Dynamic and Genetic algorithms for Multi-Input Adders.

SNo.	Benchmark Circuits	Inputs	Outputs	Initial Node Count	WIN2	WIN2ite	WIN 3	SIFT	RANDOM	Proposed GA with Crossover		
										ORDER	CYCLE	PMX
1	1-adder	3	2	8	8	8	8	8	8	8	8	8
2	2-adder	5	3	17	17	17	17	17	17	17	17	17
3	3-adder	7	4	32	32	34	32	26	34	25	32	26
4	4-adder	9	5	63	65	63	46	46	61	35	45	35
5	5-adder	11	6	126	128	126	61	55	78	49	82	44
6	6-adder	13	7	253	255	253	85	85	93	79	132	58
7	7-adder	15	8	508	510	508	94	94	264	135	165	72
8	8-adder	17	9	1027	1001	1001	287	283	845	558	396	267

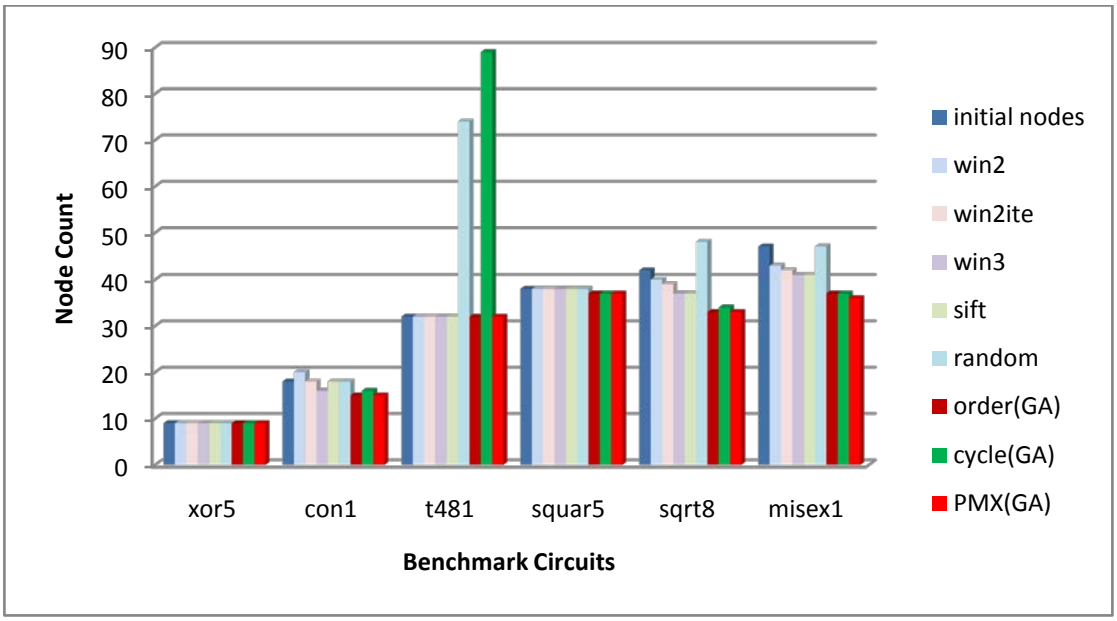

Fig6 Comparison of Node Count for different LGSynth93 Benchmark Circuits using different Algorithms.

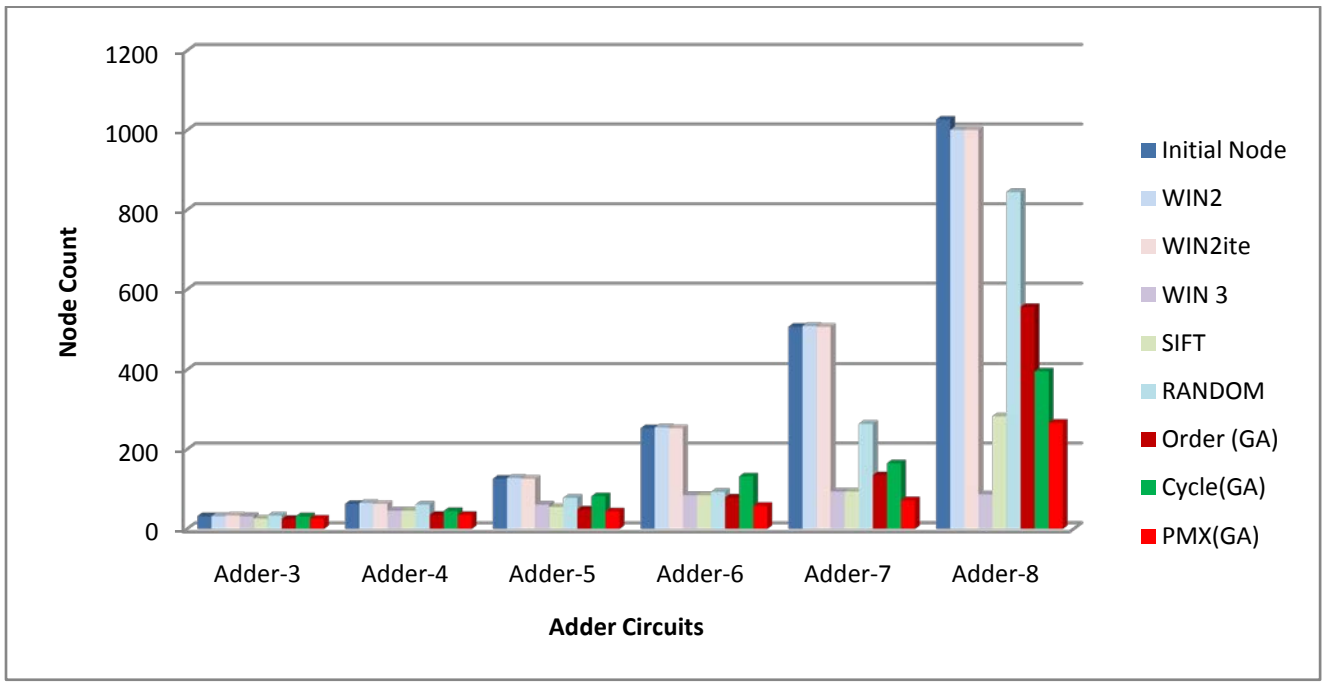

Fig7 Comparison of Node Count for multi-input adder circuits using different algorithms.

References

[1] Sheldon B. Akers.Binary Decision Diagrams,IEEE Transactions on Computers, C-27(1978).

[2] R. E. Bryant.Graph-based algorithms for Boolean function manipulation.IEEE Transactions on Computers,35 (1986).

[3] F. Towhidi, A.H. Lashkari, R.S. Hossein.Binary Decision Diagram (BDD).International Conference on Future Computer and Communication(2009) 496-499.

[4] P. W. C. Prasad, A. Assi, A. Harb and V. C. Prasad.Binary Decision Diagrams: An Improved Variable Ordering using Graph Representation of Boolean Functions.International Journal of Computer Science, 1(2006)1-7.

[5] Pinaki Mazumdar,Elizabeth M. Rudnick:Genetic Algorithms for VLSI Design,Layout and Test Automation.

[6] William N.N. Hung, Xiaoyu Song, El Mostapha Aboulhamid, and Michael A. Driscoll.BDD Minimization by Scatter Search.IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, 21 (2006).

[7] N. Zhuang, M.S.T. Benten, and P.Y.K Cheung.Improved Variable Ordering of BDDs with Novel Genetic Algorithm.IEEE International Symposium on Circuits and Systems, 3(1996)12-15.

[8] Saurabh Chaudhary, and Anirban Dutta.Algorithmic Optimization of BDDs and Performance Evaluation for Multi-level Logic Circuits with Area and Power Trade-offs. IEEE International Conference on Electronics, Circuits and Systems,(2011).

[9] Misagh Takapoo, and M.B Ghaznavi-Ghoushchi.IDGBDD: The novel use of ID3 to improve Genetic algorithm in BDD reordering.International Conference on Electrical Engineering / Electronic Computer Telecommunication and Information Technology,(2010)19-21.

[10] Tom V Mathew: Genetic Algorithm:Report submitted at IIT Bombay.

[11] Harsh Arora, Arindam Banerjee, Rahul Roopchand Jidge.Heuristic Approach to Variable Ordering for Logic Synthesis Engine Design:Algorithmic Insight.International Journal of Circuits and Architectural Design,Vol1,No.2014.

	**Manu Bansal** received her master's degree in Electronics and Communication at Thapar Institute of Engineering & Technology, Patiala (Deemed University) in 2003. She works now as Assistant Professor in Electronics & Communication Engineering Department at Thapar University, Patiala. Her research interests are CAD for VLSI, Digital VLSI Design, and Behavioral Modeling for different application fields.
	**Dr Alpana Agarwal** received her MTech Degree in Solid State Materials from IIT, Delhi in 1988 and PhD Degree at Thapar University, Patiala in 2010. She is employed as Associate Professor in Electronics & Communication Engineering Department at Thapar University, Patiala. Her research interests are VLSI Design, Design Automation, ASIC Design, Low Power Low Noise VLSI Circuit Design.